SPECIFICATION FOR APPROVAL

CUSTOMER: 标品

CUSTOMER NO.:

MODEL NO.: GW-CRPS800N2

P/N .: 5175851

APPROVAL REV.: 1

DATE: 2019.12.31

CUSTOMER AUTHORIZED SIGNATURE			
CUSTOMER	**ACCEPTED**	**CHECKED**	**APPROVED**

Please return to us on copy of "SPECIFICATION FOR APPROVAL"
with your approved signature.

SUPPLIER	DRAFTED	CHECKED	APPROVED
	Jiwu jia	Wei yang	Changbin huang

China Greatwall Technology Group Co.,Ltd Power Supply Division.
Great wall Industry Park, Baoshi East Rd, Shiyan Country, Baoan, Shenzhen
TEL: 0755--83752759 FAX: 0755--82501749

MODIFY HISTORY

NO.	Date	Description	Drafted	Approved
1	2019.12.31	Origin issue	Jiwu jia	Changbin huang
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				

CONTENTS

1 General

This specification defines the functional requirements of the switching power supply. It is a redundant server power supply with features support hot plug N+M (N=2 max, M=2 max), dual outputs (+12V and +12VSB), AC input auto ranging with power factor corrected, and internal fan(s) for force air cooling.

2 Mechanical Overview

The physical size of the power supply is 40 (H) x 73.5 (W) x 185 (L) in milli-meter. The power supply contains a single 40mm fan and incorporates a card edge output that interfaces with a 2x25 card edge connector in the system. The AC power cord plugs directly into the external face of the power supply.

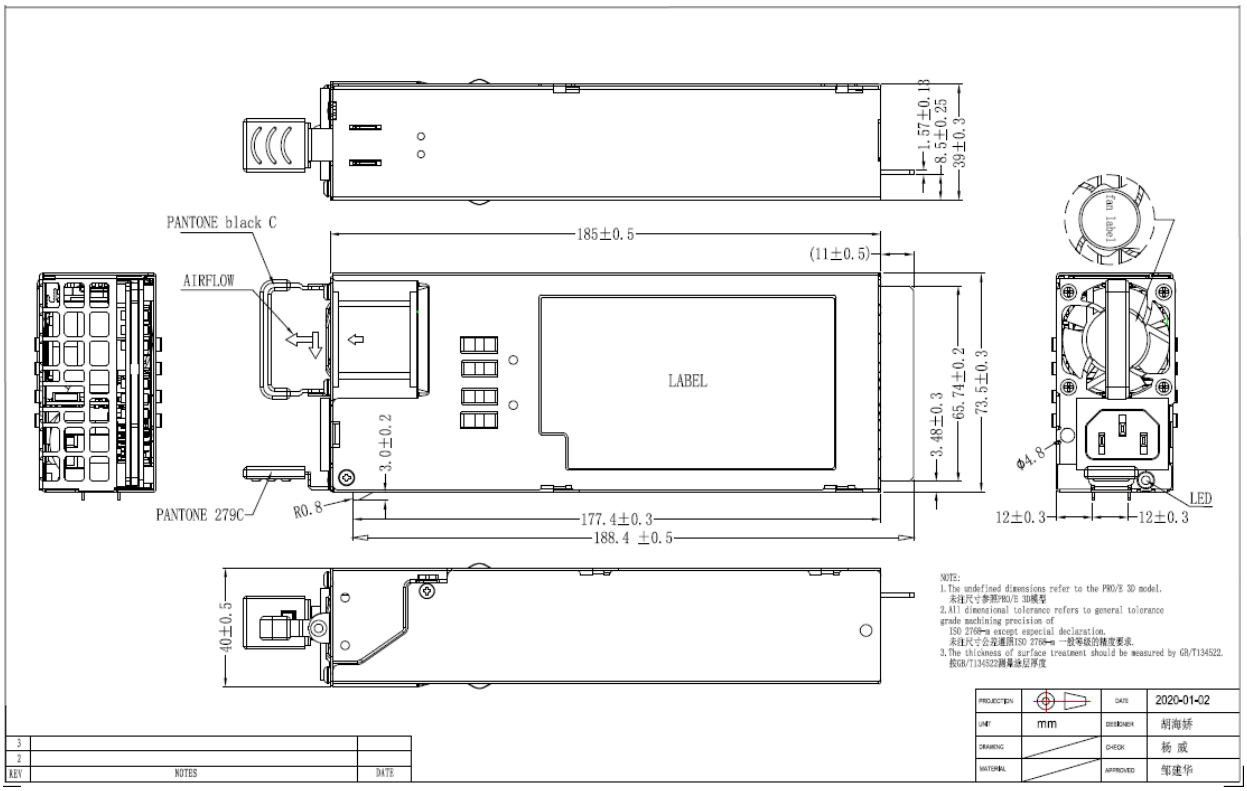

Figure 1 Shape

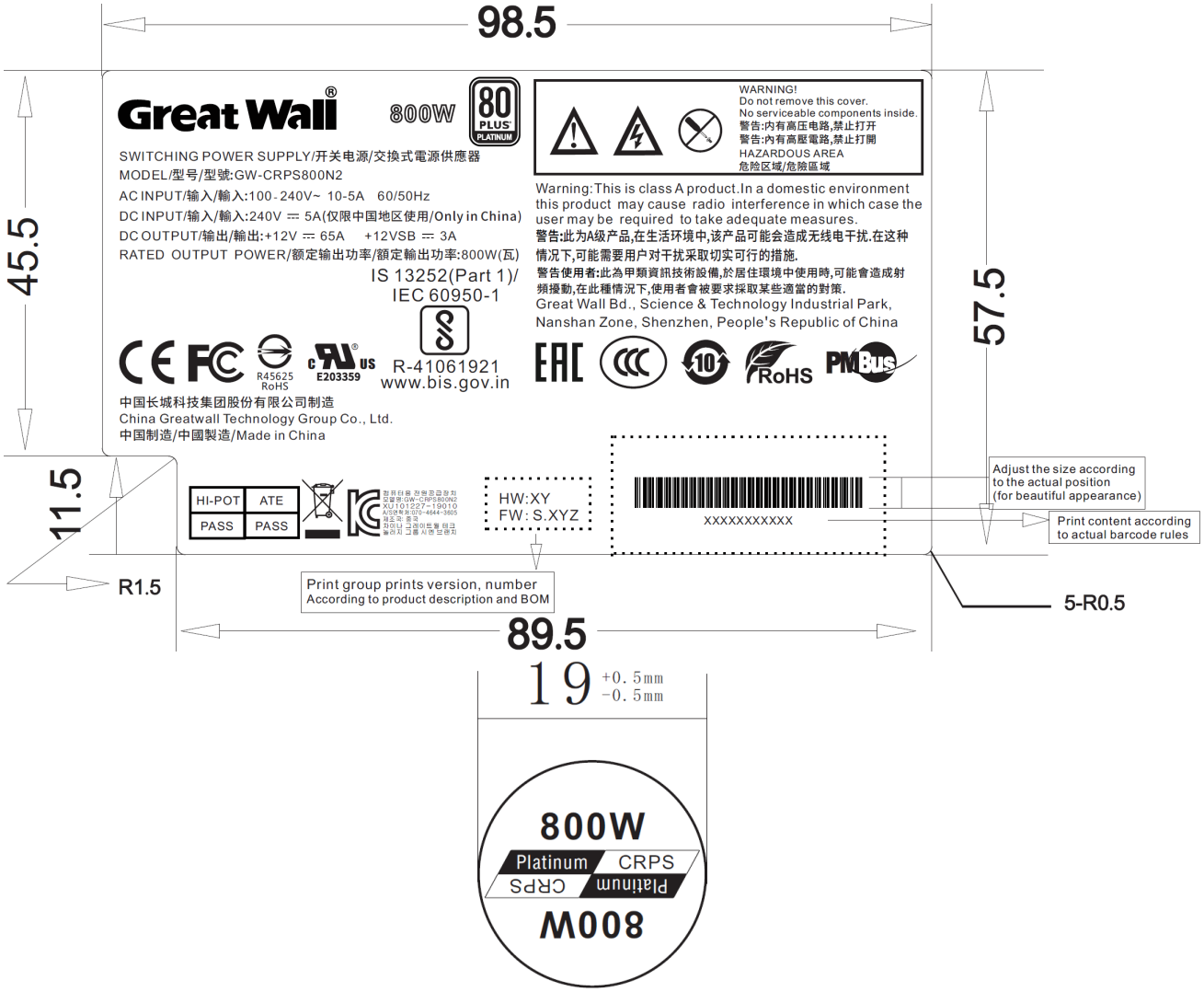

Figure 2 Example Label Illustrating Regulatory Marks

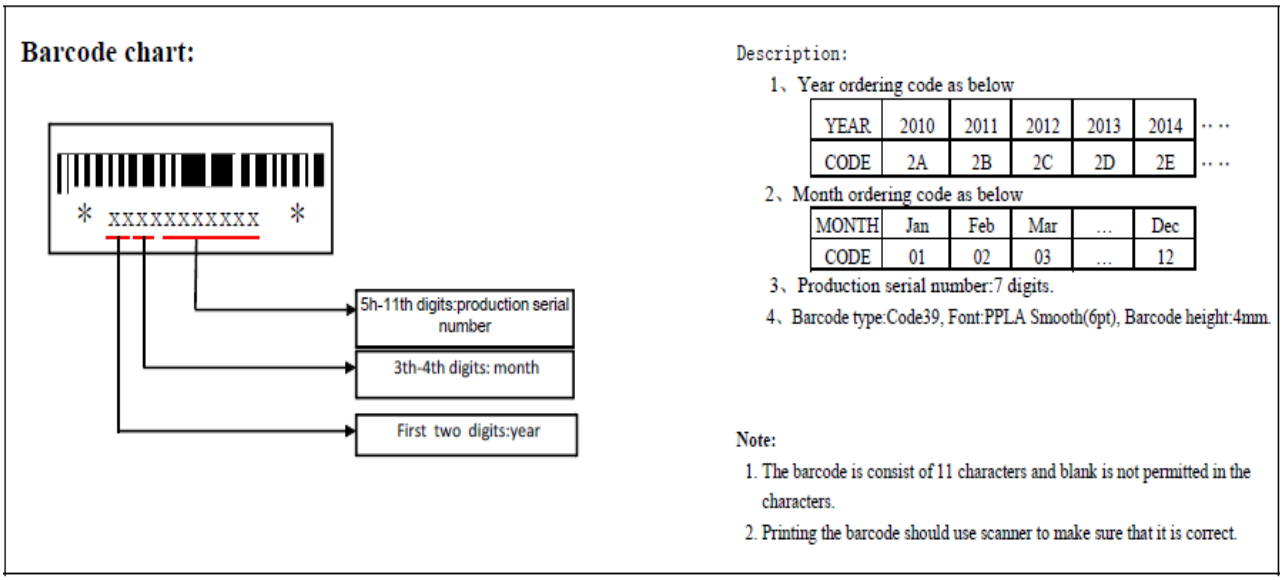

Figure 3 Bar code and label Spec

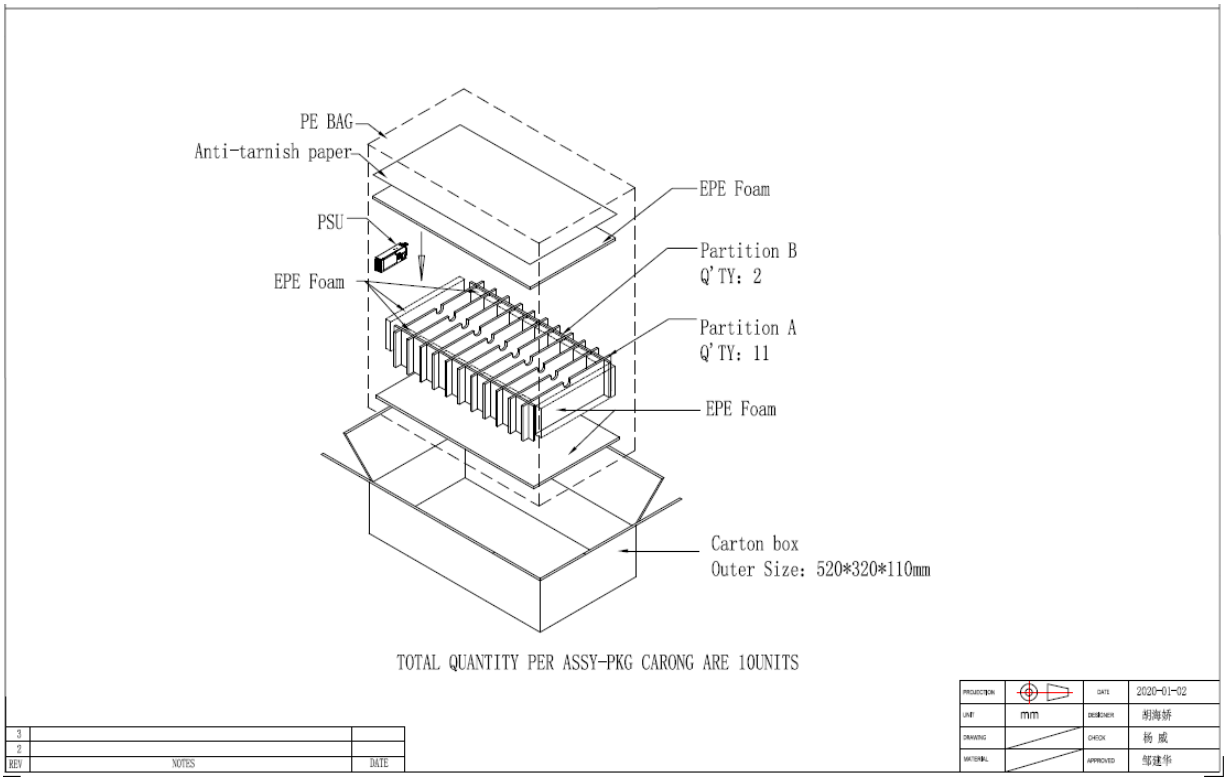

Figure 4 Packing Diagram

2.1 DC Output Connector

The power supply uses a card edge output connection for power and signal that is compatible with a 2x25 Power Card Edge connector. Table 1 defines each output pin assignment on the output connector.

Table 1 Output Pin Assignment

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	GND	B2	GND
A3	GND	B3	GND
A4	GND	B4	GND
A5	GND	B5	GND
A6	GND	B6	GND
A7	GND	B7	GND
A8	GND	B8	GND
A9	GND	B9	GND
A10	+12V	B10	+12V
A11	+12V	B11	+12V
A12	+12V	B12	+12V
A13	+12V	B13	+12V
A14	+12V	B14	+12V
A15	+12V	B15	+12V
A16	+12V	B16	+12V
A17	+12V	B17	+12V
A18	+12V	B18	+12V
A19	SDA	B19	A0 (SMBus address)
A20	SCL	B20	A1 (SMBus address)

A21	PS_ON#	B21	+12VSB
A22	SMBAlert#	B22	Cold Redundancy Bus
A23	RS-	B23	+12VLS
A24	RS+	B24	PS_PRESENT#
A25	PSOK	B25	VIN_GOOD

2.2 Airflow Direction

The power supply is designed for supporting bi-airflow directions cooling purpose. The normal airflow means the air enters the PSU at DC output side and exits through the AC inlet side. The reverse airflow means the air enters the PSU at AC inlet side and exit through the DC output side.

2.3 Handle Retention

The power supply has a handle to assist extraction. The module is able to be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extra ted from the system when the AC power cord was plugged into the power supply.

2.4 LED Indicator

The power supply uses a bi-color LED: Amber and Green to identify different operating states of the power supply. Table 2 defines the characteristics of the LED indicator.

Table 2 LED Characteristics

Power Supply Condition	LED State
Output ON and OK.	GREEN
No AC power to all power supplies.	OFF
PSU standby state AC present / Only +12VSB on (PS off) or PSU in standby state as defined in the Cold Redundancy section of the CRPS Common Requirements Specification.	1Hz Blinking GREEN
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER
Power supply critical events causing a shutdown; Failure, OCP, Short Circuit, OVP, Fan Failure, OTP, Input OVP.	AMBER
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blinking AMBER
Power supply FW updating.	2Hz Blinking GREEN

2.5 Acoustic

The power supply shall incorporate variable speed fan(s). Sound power must be measured according to ECMA 74 (www.ecma-international.org) and reported according to ISO 9296.

Table 3 PSU Sound Power Level

Load (%)	Altitude (M)	Ambient (°C)	LWA (BA)
20	900	35	TBD
60	900	40	TBD
100	900	50	TBD

3 AC Input Requirements

3.1 Power Factor and iTHD

The power supply must meet the power factor and current iTHD requirements that within Energy

Star® Program Requirements for Computer Servers.

Table 4 Power Factor Requirements

Output power	10%load	20%load	50%load	100%load
Power Factor	>0.90	>0.96	>0.98	>0.99
Input conditions	200Vac to 240Vac, 50Hz/60Hz& 115Vac, 60Hz			

Table 5 iTHD Requirements

% of Rated Load	> 5% & ≤ 10%	> 10% & <20%	≥ 20%	≥ 40%	≥ 50%
Max. iTHD (%)	< 20%	< 15%	≤ 10%	≤ 8%	≤ 5%
Input conditions	200Vac to 240Vac, 50Hz/60Hz				

Tested according to Generalized Internal Power Supply Efficiency Testing Protocol Rev6.7.
This is posted at https://plugloadsolutions.com/80pluspowersupplies.aspx.

3.2 AC Inlet Connector

The AC input connector shall be an IEC 60320 C-14 power inlet. This inlet is rated for a minimum of 10A at 250Vac. (Black color)

3.3 Input Voltage

The power supply must operate within all specified limits over the range shown in Table 6. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits. The application of an input voltage below the minimum specified in Table 6 shall not cause damage to the power supply, including fuse failure.

Table 6 Input Voltage Range

AC Line Input	Min.	Rated	Max.	Start Up	Power Off
Voltage Low Line (Vac)	90	100-127	140	85±4	74 ±5
Voltage High Line (Vac)	180	200-240	264	N/A	N/A
Frequency (Hz)	47	50/60	63	N/A	N/A
DC Input Voltage (Vdc)	180	240	310	175 ±4	165 ±5

Note: The power supply shall build in a minimum 3Vac hysteresis such that the power supply will not oscillate on and off under AC input Start Up and Power Off condition.

3.4 AC Line Dropout / Holdup Time

An AC line dropout is defined to be when the rated AC input drops to 0Vac at any phase of the AC line for any length of time. During an AC dropout the power supply shall meet dynamic voltage regulation limits. An AC line dropout of any duration shall not cause malfunction of control signals or protection circuits other than the SMBAlert# signal. If the AC dropout lasts longer than the holdup time, the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirements over rated AC voltages, frequencies and output loading conditions. A dropout of the AC line for any duration shall not cause damage to the power supply.

Table 7 AC Line Dropout / Holdup Time limits

70% Load
>10msec

3.4.1 AC Line +12VSB Holdup Time

The +12VSB output voltage shall stay in regulation under its full load (static or dynamic) during an AC dropout duration up to 70msec whether the power supply is in ON or OFF state (PS_ON# asserted or de-asserted).

3.5 AC Line Fuse

The power supply incorporates a fast blow type fuse at AC input side. AC inrush current and all protection circuits, including DC output overload or shorted output conditions, in the power supply shall not cause the AC line fuse to open under any condition.

3.6 AC Inrush

When input power is applied to the power supply, the Maximum AC line inrush Current shall not exceed 30A peak and do not concern due to Xcap current at cold start. The PSU shall meet this inrush limit for any AC voltage, during turn ON at any phase of AC voltage and over the specified temperature range.

3.7 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” will be defined as the AC line voltage dropping below rated voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above rated voltage.

Table 8 AC Line Sag Transient Performance

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
0 to 1/2 AC cycle	95%	Rated AC Voltage ranges	50/60Hz	No loss of function or performance
> 1 AC cycle	>30%	Rated AC Voltage ranges	50/60Hz	Loss of function acceptable, self-recoverable

Table 9 AC Line Surge Transient Performance

AC Line Surge (10sec interval between each surging)				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Rated AC Voltages	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	Mid-level of rated AC Voltages	50/60Hz	No loss of function or performance

3.8 Input Over Voltage Protection

The power supply shall be protected itself from input over voltage conditions caused by excessive voltage from the input power source which could cause internal part failures. When the power supply observes an input voltage which exceeds 290±4Vac or 340±4Vdc, the power supply shall disable its output and report an input over voltage fault. The supply shall re-enable its output when the input voltage falls below 280±5Vac or 330±5Vdc.

3.9 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an internal EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 10 Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended, No degradation of performance.
B	The apparatus shall continue to operate as intended, No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.10 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015 using the EN61000-4-2:2009 and IEC 61000-4-2: 2008 test standard and performance criteria B defined in Table 10.

3.11 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015 using the EN61000-4-4: 2012 and IEC 61000-4-4: 2012 test standard and performance criteria B defined on Table 10.

3.12 Radiated Immunity

The power supply shall comply with the limits defined in EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015 using the EN61000-4-3: 2006 +A1: 2008 +A2: 2010 and IEC 61000-4-3: 2006 _A1: 2007 +A2: 2010 test standard and performance criteria A defined on Table 10.

3.13 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave; ±2kV line to earth and ±1kV line to line, per EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015, EN61000-4-5: 2014 and IEC 61000-4-5: 2014.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels. No change in operating state or loss of data during and after the test profile. No component damage under any condition.

Note: The power supply shall be tested to ±2.6kV line to earth and ±1.3kV line to line to check for design margin.

The power supply shall comply with the limits defined in EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015 using the EN61000-4-5: 2014 and IEC 61000-4-5: 2014 test standard and performance criteria B defined on Table 10.

3.14 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024:2010 +A1:2015 and CISPR 24:2010 +A1:2015 using the IEC61000-4-11: 2004 and IEC 61000-4-11: 2004 test standard and performance criteria C defined on Table 10.

3.15 Power Recovery

The power supply shall recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

4 Efficiency

The following table shows the minimum efficiency requirements according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7 at 230Vac & 240Vdc and 25°C conditions excluded the losses of PSU fan. Total power is defined as 800W, meanwhile +12V can reach 65.0A.

Table 11 PSU Efficiency

Efficiency	10% Load	20% Load	50% Load	100% Load
Platinum Plus	88%	90%	94%	91%

5 DC Output Specification

5.1 Output Power / Currents

The following table defines the power supply output current rating. The power supply shall meet both static and dynamic voltage regulation limits for all conditions. No damaged shall be occurred under no load condition at all inputs defined in Table 6 and any operating ambient conditions.

Table 12 Output Current rating

Parameter	Input Range	Min. Current	Max. Current
+12V	90Vrms-264Vrms/ 180VDC-310VDC	1A	65.0A
+12VSB	90Vrms-264Vrms/ 180VDC-310VDC	0.1A	3.0A

Table 13 Peak Load Requirements

Output	Input voltage (Vac)	CLST Peak 20sec duration[2] (A)	Pmax.app Peak 10msec duration[3] (A)	Pmax Peak 100μsec duration[4] (A)
+12V	200-240	Max rating + 6A	Max rating + 30A	Max rating + 45A
+12V	100-127	Max rating + 6A	Max rating + 30A	Max rating + 45A
+12VSB[1]	100-240	Max rating + 0.3A	NA	NA

Note:

1. +12VSB must provide 4.0A with two power supplies in parallel.
2. Close Loop System Throttling (CLST) Peak load duration is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20sec without asserting the SMBAlert# signal at maximum operating temperature.
3. Pmax.app peak duty cycle shall be 5%; 10msec at Pmax.app peak / 200msec at rated current. Applying a Pmax.app peak load must not trip the SMBAlert# signal. The maximum length of time the Pmax.app peak must be supported is based on the SMBAlert# signal asserting. The PSU must support this peak load for 5msec after SMBAlert# asserts.
4. Pmax peak must be support based on PMAX Protection requirements that included added system +12V capacitors. Apply loading greater than Pmax.app load may trip the SMBAlert# signal for quickly throttling the processor and memory load. See section 5.2 for details.

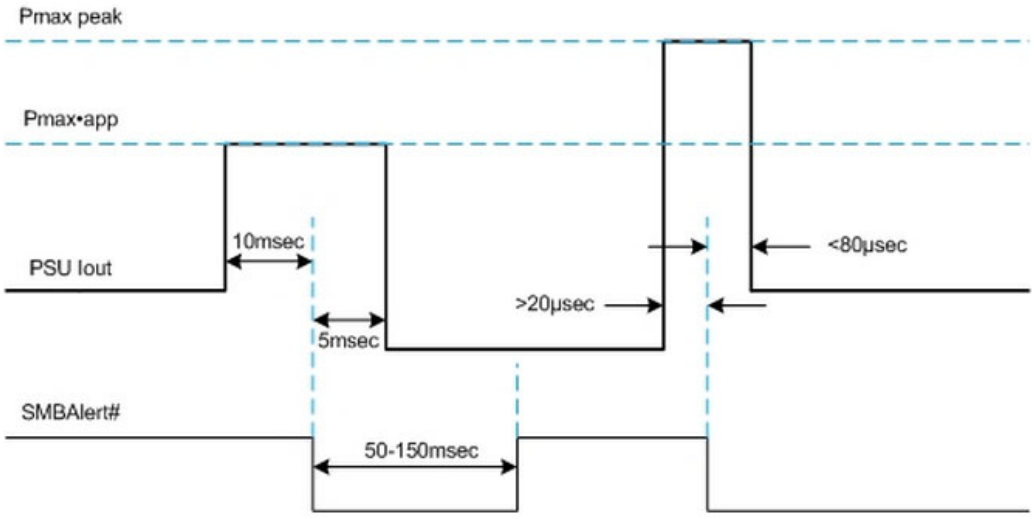

Figure 5 PSU Peak Timing

5.2 Pmax Peak Load Protection Requirements

For peak loads above the Pmax.app peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 100µsec. For peak loads up to Pmax.app peak load level the PSU must not assert SMBAlert# if the peak load duration is <10msec. If the peak load last longer than 10msec the PSU may assert SMBAlert# to throttle the load within 15msec.

Table 14 PMAX Protection testing Conditions

Pmax Peak Load	Peak Current	System Capacitance	SMBAlert # Timing	Peak Load Duration	Voltage Undershoot
Max rating +540W	Max rating +45A	6 x 1,500µF	< 5msec	100µsec	-2%

5.3 Standby Output

The +12VSB output shall present when AC input greater than the power supply start up voltage. There should be load sharing in the standby rail.

5.4 Voltage Regulation

The power supply output voltages shall stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple & noise. These shall be measured at the output connectors.

Table 15 Voltage Regulation Limits

PARAMETER	TOLERANCE	MIN	NOM	MAX	UNITS
+12V	- 5% / +5%	+11.6	+12.2	+12.8	Vrms
+12VSB	- 5% / +5%	+11.6	+12.2	+12.8	Vrms

5.5 Dynamic Loading

The output voltages shall remain within limits specified in Table 16 for the step loading and capacitive loading. The load transient repetition rate shall be tested between 10Hz and 5KHz at duty cycles ranging from 10% to 90%. The step load may occur anywhere within the MIN load to the Peak load conditions.

Table 16 Transient Load Requirements

Output	Step Load Size	Load Slew Rate	Test with Capacitive Load
+12V	60% of max load	0.5 A/μsec	1000 μF
+12VSB	1.0A	0.5 A/μsec	1000 μF

5.6 Capacitive Loading

The power supply shall be stable and meet all limits with the following capacitive loading ranges which shown in Table 17.

Table 17 Capacitive Loading Conditions

Output	MIN	MAX	Units
+12V	2000	50000	μF
+12VSB	10	3100	μF

Note: The minimum capacitive load on +12V output is required to hold regulation during Cold Redundancy mode power supply failure and power supply hot swapping.

5.7 Grounding

The output ground (GND) pins of the power supply provide the output power return path. And all the GND pins are connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

5.8 Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 5.6. A minimum of: 30 degrees phase margin and -6dB gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

5.9 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 300mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

5.10 Common Mode Noise

The Common Mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 150MHz.

The measurement shall be made across ground at the DC power connector and chassis ground (power subsystem enclosure).

The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.11 Soft Starting

The power supply contains a control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

5.12 Zero Load Stability Requirements

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.13 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply used a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

5.14 Load Sharing

The +12V output will have active load sharing. The output will share within 10% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations. +12VSB output is not required to actively share current between power supplies (passive sharing). The +12VSB output of the power supplies are connected together in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

5.15 Ripple / Noise

The maximum ripple/noise output of the power supply is defined in Table 18.
This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors and with a minimum capacitive loading (refer to Table 17) on each of output. A 10μF ceramic capacitor in parallel with a 0.1μF ceramic capacitor is placed at the point of measurement.

Table 18 Ripple and Noise

+12V	+12VSB
120mVp-p	120mVp-p

5.16 Timing

Figure 2 and Table 19 define the timing sequence for the power supply operation. Both +12V and +12VSB outputs shall rise monotonically. Table below shows the timing requirements for the power supply being turned on and off two different ways; 1) via the AC input with PSON held low; 2) via the PSON signal with the AC input applied.

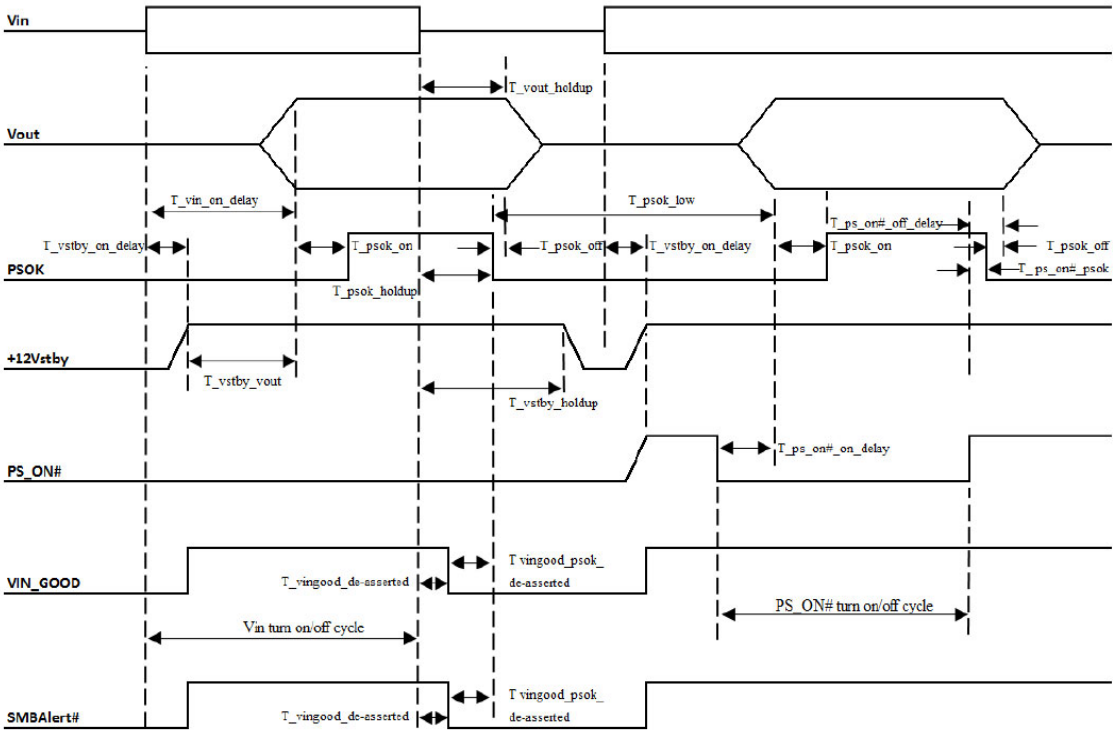

Figure 6 Turn On/Off Timing

Table 19 Power Supply Timing Requirements

Item	Description	MIN	MAX	UNITS
$T_{\_vout\_rise}$	Output voltage rise time for +12V and +12VSB from 10% to within regulation limits.	5	70	ms
$T_{\_vstby\_on\_delay}$	Delay from AC being applied to +12VSB being within regulation.		1500	ms
$T_{\_vin\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		3000	ms
$T_{\_vout\_holdup}$	Time +12V output voltage stay within regulation after loss of AC.	11		ms
$T_{\_psok\_holdup}$	Delay from loss of AC to de-assertion of PSOK.	10		ms
$T_{\_ps\_on\#\_off\_delay}$	Delay from PS_ON# de-asserted to power supply turning off.		10	ms
$T_{\_ps\_on\#\_on\_delay}$	Delay from PS_ON# active to output voltages within regulation limits.	5	400	ms
$T_{\_ps\_on\#\_psok}$	Delay from PS_ON# deactivate to PSOK being de-asserted.		5	ms
$T_{\_psok\_on}$	Delay from output voltages within regulation limits to PSOK asserted at turn on.	100	500	ms
$T_{\_psok\_off}$	Delay from PSOK de-asserted to output voltages dropping out of regulation limits.	1		ms
$T_{\_psok\_low}$	Duration of PSOK being in the de-asserted state during an off/on cycle using AC or the PS_ON# signal.	100		ms
$T_{\_vstby\_vout}$	Delay from +12VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
$T_{\_vstby\_holdup}$	Time the +12VSB output voltage stays within regulation after loss of AC.	70		ms
$T_{vingood\_de-asserted}$	Delay from the Vin drop being 0V to VIN_GOOD de-assertion. (and SMBAlert# low)		3	ms

6 Protection Circuits

Protection circuits inside the power supply shall only cause the power supply's main outputs to shut down. The power supply will latch off after auto-recovering 3 times. The power supply latches off due to a protection circuit tripping, an AC cycle OFF or a PS_ON# cycle HIGH shall be able to reset the power supply.

6.1 Over Current Warning, Over Current Protection & Over Power Protection (OCW, OCP & OPP)

The power supply shall have over current protection (OCP), over current warning (OCW), and over power protection (OPP) limits as defined in below table. These are defined to protect the PSU and to allow peak currents to power the system without PSU shutting down.

Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the PSU but also to allow peak current to the system without throttling the system.

When OCP trips, it shall shut down and latch OFF the PSU. This latch shall be cleared by toggling the PS_ON# signal or by an AC power interruption (Except the +12VSB protection occurred). The power supply shall not be damaged from repeated power cycling on this condition.+12VSB will be auto-recovered after removing OCP limit.

Table 20 Over Current Protection

Spec	Description	Thresholds		Timing	
		MIN	MAX	MIN	MAX
OPP/Fast OCP	Over power protection	Rating +40A	Rating +45A	100μsec	
Slow OCP	Slow over current protection	Rating +6A	Rating +30A	20msec	500msec
Fast OCW	Fast over current warning (SMBAlert#)	Rating +40A	Rating +45A	20μsec	5msec
Slow OCW	Slow over current warning (SMBAlert#)	Rating +6A	Rating +30A	10msec	15msec
OCPstby	Stby over current protection (hiccup mode)	3.5A	9A	1msec	100msec

Note: Fast OCW/Slow OCW must before the OPP/Fast OCP/Slow OCP occurred.

6.2 Fast Output Current sensing

The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the over power protection threshold in the PSU. The SMBAlert# signal must always assert before the over power protection threshold is exceeded. SMBAlert# must always latch for about 100msec before being released. The requirements are stated in Table 19.

6.3 Over Power Protection (OPP)

The power supply shall support over power protection (OPP) level low enough to protect the power supply running in this mode for repeated 0.1msec durations at a 1% duty cycle. The power supply shall be stable operating at any load point from rated power up to the OPP point.

6.4 Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the

PS_ON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels defined in Table 21 when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. +12VSB will be auto-recovered after removing OVP limit.

Table 21 Over Voltage Protection (OVP) Limits

Output Voltage	Min. (V)	Max. (V)
+12V	13.5	15.5
+12VSB	13.5	15.5

6.5 Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the +12VSB remains always on. The OTP circuit has built in a margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level shall be at least 5°C higher than SMBAlert# over temperature warning threshold level.

7 Control Signals and PMBus Reporting Accuracy

The following sections define the input and output signals from the power supply.
Signals that can be defined as low active use the following convention: Signal# = low active

7.1 PS_ON# Input Signal (Pin A21)

The PS_ON# signal is required to remotely turn on/off the power supply. PS_ON# is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +12VSB) turn off.
This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. Refer to Table 22 for the PS_ON# signal characteristics.

Table 22 PS_ON# Signal Characteristics

Signal Type (Active Low)	**Accepts an open collector/drain input from the system. Pull up to 3.3Vstby located in the power supply.**	
PS_ON# = Low	ON	
PS_ON#= High or Open	OFF	
	Min.	Max.
Logic level low (power supply ON)	0V	0.4V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, PS_ON# = Low		4.0 mA
PS_ON# rise and fall time		100μsec

7.2 PSOK (Power OK, Pin A25)

PSOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PSOK will be de-asserted to a LOW state. The start of the PSOK delay time shall inhibited as long as any power supply output is in current limit. Refer to Table

23 for the PSOK signal characteristics.

Table 23 PSOK Signal Characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to 3.3Vstby located in the power supply.**	
PSOK = High	Power OK	
PSOK = Low	Power Not OK	
	Min.	Max.
Logic level low voltage	0V	0.4V
Logic level high voltage	2.4V	3.46V
Sink current, PSOK = low		400μA
Source current, PSOK = High		2mA
PSOK rise and fall time		100μsec

7.3 SMBAlert# (Pin A22)

This is an active low signal and indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of the critical component temperature reached a warning threshold, over-current, over voltage, under voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Amber or blink Amber. Refer to Table 24 for the SMBAlert# signal characteristics.

Table 24 SMBAlert# Signal Characteristics

Signal Type (Active Low)	**Open collector/drain output from power supply. Pull-up to 3.3Vstby located in the system.**	
SMBAlert# = High	Power OK	
SMBAlert# = Low	Power Not OK	
	Min.	Max.
Logic level low voltage	0V	0.4V
Logic level high voltage	2.4V	3.46V
Sink current, SMBAlert# = Low		4mA
Source current, SMBAlert# = High		80μA
SMBAlert# rise and fall time		100μsec

7.4 RS- (Return Remote Sense, Pin A23)

The power supply has return remote sense (RS-) to regulate out ground drops in the system for the main output voltage.

Refer to Sec. 5.14 Load Sharing.

7.5 RS+ (+12V Remote Sense, Pin A24)

The power supply uses +12V remote sense (RS+) to regulate out +12V drops in the system for the main output voltage.

Refer to Sec. 5.14 Load Sharing.

7.6 Cold Redundancy Bus (Pin B22, enable by system)

This pin is used in the Cold Redundancy mode control which all of Cold Redundancy Bus signals should be tied together. When the pin is HIGH in the Cold Redundancy mode, the slave power supply

will enter the Cold Standby mode (sleep mode, +12V and +12VSB no output); and when the pin is LOW, the Cold Standby mode power supplies will in normal redundancy mode.
Cold Redundancy feature supports 1+1, 2+1, 3+1 and 2+2 redundant configurations. It uses the PMBus manufacturer specific command area to define PMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

7.7 PS_PRESENT# (Pin B24)

This signal is an active low type signal and is connected to the power supply's output ground internally. The mating pin of this signal in system side should have a pull-up resistor which limit the max. current 4mA to go through from this signal pin to the power supply. A LOW state on this signal indicates the PSU is physically presents.

7.8 VIN_GOOD (Pin B25)

The VIN_GOOD signal indicates that input voltage is applied to the power supply and that the input voltage meets the requirements of section 3.3. Within 3ms after the input voltage drop to 0V the VIN_GOOD must be driven LOW. In parallel mode the VIN_GOOD signal is always LOW at that power supply which has no input.

Table 25 VIN_GOOD Signal Characteristics

Signal Type (Active High)	**Open collector/drain output from power supply. Pull-up to 3.3Vstby located in the power supply.**	
VIN_GOOD = High	Input voltage ok	
VIN_GOOD = Low	Input voltage failure	
	Min.	Max.
Logic level low voltage,	0V	0.4V
Logic level high voltage,	2.0V	3.46V
VIN_GOOD asserted		81~89Vac 171~179Vdc
Sink current		1mA
Source current		3.3mA
VIN_GOOD rise and fall time		100μsec

7.9 SDA (Pin A19)

SMBus Data: Pull-up to PSU internal +3.3Vstby via 10k-ohm resistor.

7.10 SCL (Pin A20)

SMBus Clock: Pull-up to PSU internal +3.3Vstby via 10k-ohm resistor.

7.11 A0 (Pin B19)

Address Bit 0: Pull-up to PSU internal +3.3Vstby via 10k-ohm resistor.

7.12 A1 (Pin B20)

Address Bit 1: Pull-up to PSU internal +3.3Vstby via 10k-ohm resistor.

7.13 +12VLS (Pin B23)

This pin supports an active current sharing function for main output +12V by connecting all the

+12VLS signals together.
Refer to Sec. 5.14 Load Sharing.

7.14 PMBus Reporting Accuracy

Table 26 defines the accuracy under rated AC input ranges for PSU.

Table 26 PMBus Accuracy

	Accuracy（110Vac or 220Vac or 270Vdc）
Load	＞10%
READ_VIN	±3%
READ_IIN	±0.3A or±3%
READ_PIN/READ_EIN	±5W or±3%
READ_VOUT	±2%
READ_IOUT	±1A or±3%
READ_POUT/READ_EOUT	±5W or±3%
READ_SPEED_1	±2%
READ_TEMPERATURE_1	±3℃

8 Environmental Requirements

8.1 Temperature

Operating: 0~ 55°C
Non-Operating: -40 ~ 70°C

8.2 Humidity

Operating: To 85% relative humidity (non-condensing).
Non-Operating: - To 95% relative humidity (non-condensing)

8.3 Altitude

Operating: To 5000 m
Non-operating: To 15200 m

8.4 Mechanical Shock

Non-operating: 50G Trapezoidal Wave, Velocity change = 170(inch/sec).
Three drops in each of six directions are applied to each of the samples.

8.5 Random Vibration

Non-operating
Sine sweep:
5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points.
Random profile:
5Hz @ 0.01g²/Hz to 20Hz @ 0.02g²/Hz (slope up); 20Hz to 500Hz @ 0.02g²/Hz (flat); Input acceleration = 3.13gRMS; 10 min. per axis for 3 axes on all samples.

8.6 Thermal Shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C /min. ≧transition time ≧ 15°C /min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

9 FRU Requirements

9.1 FRU Data

The FRU data format shall be compliant with the IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999) specification. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

9.2 FRU Device Protocol

The FRU device will implement the protocols including the Byte Read and Sequential Read.
The information to be contained in the FRU devices is shown in the following table.

Table 27 FRU data format

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:
Field Name	Field Description
Manufacturer Name	{Formal name of manufacturer}
Product Name	{Manufacturer's model number}
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	{Not required}
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}
Multi-Record Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply: Power Supply Information (Record Type 0x00) DC Output (Record Type 0x01) No other record types are required for the power supply. Multi-Record information shall be defined as follows:
Field Name (PS Info)	Field Information Definition
Overall Capacity (watts)	800W
Peak VA	880W
Inrush current (A)	30
Inrush interval (msec)	5
Low end input voltage range 1	90
High end input voltage range 1	140
Low end input voltage range 2	180
High end input voltage range 2	264
Low end input frequency range	47Hz
High end input frequency range	63Hz
A/C dropout total. (msec)	10
Binary flags	Set for: Hot Swap support, Auto switch, and PFC
Peak Wattage	880W
Combined wattage	None
Predictive fail tach support	Supported
Field Name (Output)	Field Description: Two outputs are to be defined from #1 to #2, as follows: +12V and +12VSB.
Output Information	Set for: Standby on +12VSB, No Standby on all others.
All other output fields	Format per IPMI specification, using parameters in this specification.

Table 28 FRU data

	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F
0x00	1	0	0	0	1	9	0	F5	1	8	0	CA	47	52	45	41
0x10	54	20	57	41	4C	4C	CC	43	52	50	53	38	30	30	4E	32
0x20	20	20	20	CC	43	52	50	53	38	30	30	4E	32	20	20	20
0x30	C3	31	2E	32	CF	20	20	20	20	20	20	20	20	20	20	20
0x40	20	20	20	20	C0	C0	C1	2E	0	2	18	52	94	20	3	70
0x50	3	1E	0	28	23	20	67	28	23	20	67	2F	3F	7	E	20
0x60	B3	0	0	0	0	1	2	D	87	69	81	C4	4	88	4	0
0x70	5	78	0	64	0	B8	B	1	2	D	53	9D	2	C4	4	88
0x80	4	0	5	78	0	F4	1	E8	FD	0	0	0	0	0	0	0
0x90	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xA0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xB0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xD0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xE0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0xF0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

stands for SN.

10 FIRMWARE Requirements

10.1 PMBus

Refer to “PMBus Application Profile for AC/DC & DC/DC Server Power Supplies, Revision 1.31” for the PMBus requirements.Related Documents

PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2

PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2 System Management Bus (SMBus) Specification Version 2.0

Addressing

The PSU PMBus device address locations are shown below. For redundant systems there are up to three signals to set the address location of the PSU once it is installed in the system; Address1, Address0. For non-redundant systems the PSU device address location should be B0h.

Table 29 PSU PMBus/IPMI FRU Address Location

Addresses used:	**Main addressing used for most server power supplies with two addressing pins**			
System addressing /Address1/ Address0	0/0	0/1	1/0	1/1
PMBus device write/read addresses	B0h/B1h	B2h/B3h	B4h/B5h	B6h/B7h
FRU device write/read addresses	A0h/A1h	A2h/A3h	A4h/A5h	A6h/A7h

1 Non-redundant power supplies will use the 0/0 address location

2 The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.

3 The ‘0’ and ‘1’ correspond to ‘0’ = signal is grounded; ‘1’ = signal is not grounded.

Hardware

The device in the power supply shall be compatible with both SMBus 2.0 ‘high power’ specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

PMBus Power Sourcing

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the OR’ing device. The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

Pull ups

Only weak pull-up resistors shall be on SCL or SDA inside the power supply. The main pull-up resistors are provided by the system and may be connected to 3.3V or 5V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

Data Speed

The PMBUS device in the power supply shall operate at the full 100 kbps.

Bus Errors

300ns maximum fall time with a 400pF capacitive load and 2.7Kohm pull up to 3.3V 10ns minimum fall time with a 20pF capacitive load and 2.7Kohm pull up to 3.3V The power supply shall not load the SMBus if it has no input power

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition

Additional SMBus hardware requirements

Writing to the power supply

When responding to read commands the power supply shall extend the clock until all writing of data to the command is complete. The power supply must still meet the Tlow: sext max time of 25msec described data speed. This is needed to make sure if the system performs a series of write and then and immediate read to the same command the power supply returns the value just written to the power supply.

Sensors

The following PMBus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC (or -36VDC to -75VDC for DC input power supplies). They shall be tested down to 10% load.

Table 30 Current / Power / Temperature Monitoring PMBus Commands

PMBus command	Description
READ_EIN	New input energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_PIN	Input power meter based on PMBus rev 1.1 spec. Uses Linear formatting.
READ_IOUT	Output current in amps for the total +12V current. The other outputs are not sensed. Uses linear format.
READ_EOUT	New output energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_TEMPERATURE_1	Returns the temperature in °C of the inlet temperature. Based on PMBus rev 1.1 spec. Uses linear format.
READ_TEMPERATURE_2	Returns the temperature in °C of the hot spot temperature. Based on PMBus rev 1.1 spec. Uses linear format.

Sensor Functionality in Different PSU States and Configurations

The functionality of READ_EIN and READ_EOUT in different PSU configurations is stated in the below table. The PSU must continue incrementing the sample counter even if AC power is not present to the PSU but the PMBus device in the PSU is powered from the other power supplies in parallel.

Table 31 READ_EIN & READ_EOUT Functioning in differing states

Number of PSUs in system	One PSU state (PSU1)	Rest of PSU states (PSUn)	PSU1 Power Accumulator	PSU1 Sample counter
1 or more	ON & AC present	All ON & AC present	New power values continue to add to the power accumulator based on loading condition	Sample counter increments every sample period
1 or more	Stby & AC present	All ON & AC present	New power values continue to add to the power accumulator based on loading condition	Sample counter increments every sample period
1 or more	OFF & no AC present	All OFF & no AC present	Reset power accumulator values to 00 when AC power is re-applied	Reset sample counter to 00 when AC power is re-applied
2 or more	AC power not present	Rest of PSUs in standby mode & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period
2 or more	AC power not present	Rest of PSUs ON & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period

READ_PIN, READ_IOUT, and READ_TEMPERTURE shall continue to report accurate values when the PSU is in standby mode or when it has no AC power but is in parallel with another PSU(s) with AC power and standby power present.

READ_PIN (97h)

The power supply shall provide input power data in watts. The data shall be reported using the PMBus linear format. The data shall be the average input power or filtered input power. If a simple average is used to provide average input power, the minimum averaging duration shall be 2 seconds.

If filtering is used; the maximum filter bandwidth shall be 0.5 Hz. The minimum accuracy shall be +/-3% over 20% to 100% load range; +/-3% over 10% to 19% load range. The accuracy shall be tested by polling with the READ_PIN command at a rate ranging from 1 sample / second to 10 samples / second.

Table 32 READ_PIN Requirements Summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The AC input power shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy 20% to 100% load	±3%		The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy 10% to 20%	5W or ±3%		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

Resetting READ_PIN
The READ_PIN power value should reset to 0W when AC power is lost.

READ_IOUT (8Ch)

The power supply shall provide output current data in amperes. The data shall be reported using the PMBus linear format. The data shall be the average output current or filtered output current. If a simple average is used to provide average output current, the minimum averaging duration shall be 2 seconds. If filtering is used; the maximum filter bandwidth shall be 0.5 Hz .The minimum accuracy is specified in the table below. The accuracy shall be tested by polling with the READ_IOUT command at a rate ranging from 1 sample / second to 10 samples / second.

Table 33 READ_IOUT Requirements Summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The output current shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy 20% to 100% load	±3%		The output current data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy 10% to 20%	1A or ±3%		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

READ_EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 34 READ_EIN Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details
Psample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate Psample.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Accuracy 20% to 100% load	±3%		The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy 10% to 20% load	5W or ±3%		
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.
IMPORTANT: The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).			

READ_EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 35 READ_EOUT Requirements Summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details
[Paccum / N] Accuracy (10% to 100% load)	5W or±3%		The calculated output power data shall meet these accuracy requirements
System polling rate	1 sample /s	10 sample /s	The PSU shall be polled over this range of rates while testing accuracy.

READ_EIN & READ_EOUT Formats

The READ_EIN and READ_EOUT commands shall use the PMBus direct format to report an accumulated power value and the sample count. The PMBus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the PMBus COEFFICIENT command. The

coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h. READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

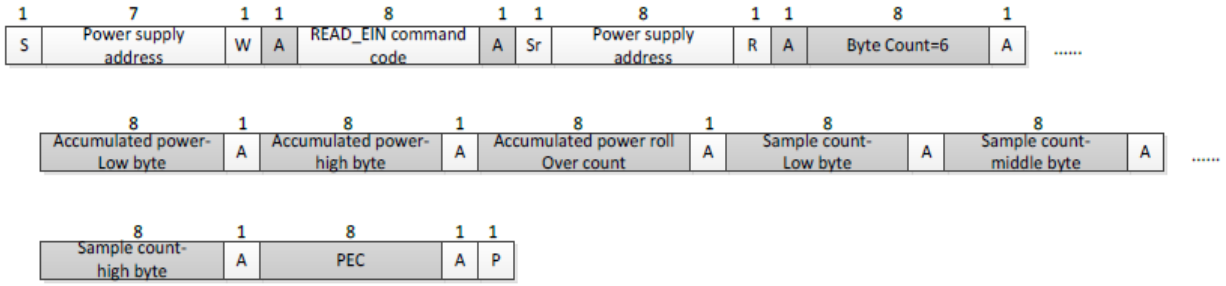

Figure 7 Read_EIN command

READ_EIN Command

READ_EIN and READ_EOUT Accumulators

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

READ_EIN PSU Functional Diagram

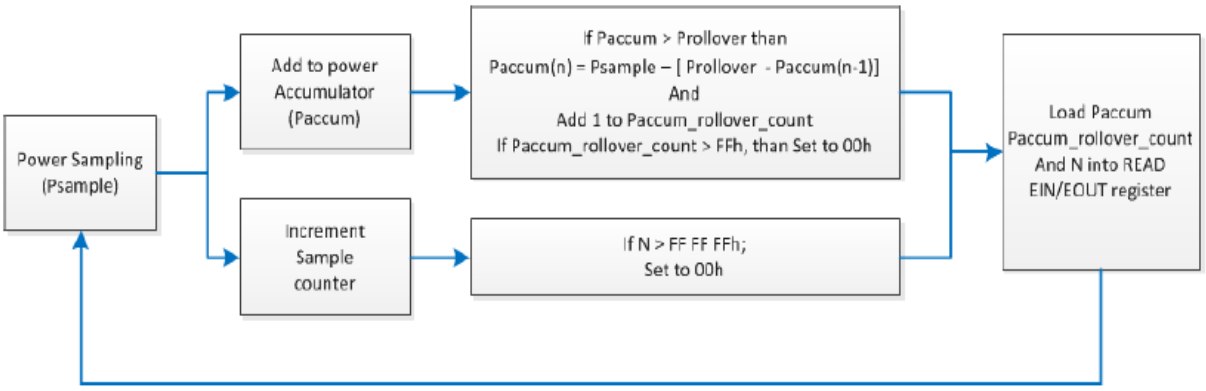

Figure 8 Read_EIN Functional Diagram

Table 36 Read_EIN Data

Psample:	**The sampled power value in linear or direct format**
Paccum:	2 bytes in PMBus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)

N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

Resetting READ_EIN

The READ_EIN and READ_EOUT power accumulator, roll-over counter, and sample count should keep the latest value when the power supply is put into standby mode. The power accumulator, roll-over counter and sample count should reset to 00 when AC power is lost long enough to cause the power supply to shutdown.

COEFFICIENT (30h)

The COEFFICIENTS command is used to retrieve the m, b and R coefficients needed by data in the DIRECT format.

The power supply shall support the PMBus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN accumulated power values.

Table 37 COEFFICIENT Data

Command	COEFFICIENTS support	m	b	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h

For the read portion of the process call, the byte count is five and the five bytes returned are (in this order):

- Lower byte of m,
- Upper byte of m,
- Lower byte of b,
- Upper byte of b,
- Single byte of R.

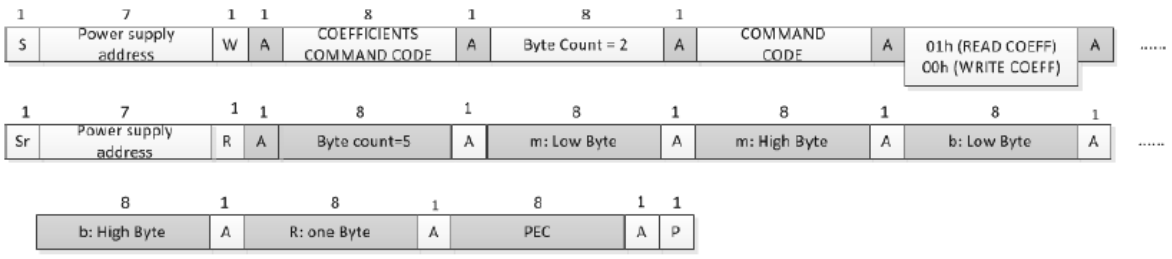

Figure 9 Retrieving Coefficients Using PEC

Status commands

The following PMBus STATUS commands shall be supported. All STATUS commands stated in Table as supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present.

Once a bit is asserted it shall stay asserted until cleared using one of the methods shown in **"Resetting of Status Bits"**. The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT#_MASK command is used to define which status event control the SMBAlert# signal. Default values for these mask bits are shown in the table below.

Table 38 PMBus STATUS Commands Summary

PMBus command	**Bit location**	**Instances No PAGE'ing 2 PAGE 00h = BMC PAGE 01h = ME**	**SMBALERT#_MASK defaults for each of the three instances(No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert#1 = does not cause assertion of SMBAlert#**
STATUS_WORD		No PAGE, 00h, 01h	NA
OFF	6 (lower)		NA
IOUT_OC_FAULT	4 (lower)		NA
TEMPERATURE	2 (lower)		NA
VIN_UV_FAULT	3 (lower)		NA
CML	1 (lower)		NA
VOUT	7 (upper)		NA
IOUT/POUT	6 (upper)		NA
INPUT	5 (upper)		NA
FANS	2 (upper)		NA
STATUS_VOUT		No PAGE'ing	
VOUT_OV_FAULT	7		1, NA, NA
VOUT_UV_FAULT	4		1, NA, NA
STATUS_IOUT		No PAGE'ing, 00h, 01h	
IOUT_OC_FAULT	7		1, 1, 1
IOUT_OC_WARNING	5		1, 1, 0
POUT_OP_FAULT	1		1, 1, 1
POUT_OP_WARNING	0		1, 1, 0
STATUS_INPUT		No PAGE'ing, 00h, 01h	
VIN_UV_WARNING	5		1, 1, 1
VIN_UV_FAULT 1	4		1, 1, 0
Unit off for low input voltage	3		1, 1, 1
IIN_OC_WARNING	1		1, 1, 1
PIN_OP_WARNING	0		1, 1, 1
STATUS_TEMPERATURE		No PAGE'ing, 00h, 01h	
OT_FAULT			1, 1, 1
OT_WARNING			1, 1, 0
STATUS_FANS_1_2		No PAGE'ing	
Fan 1 fault3			1, NA, NA
Fan 1 warning3			1, NA, NA

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.

2. 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.

3. All fans in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

Resetting of Status Bits

The STATUS_ commands shall be reset only by the below methods.

If the event is still present that caused the assertion of the status bit, the bit shall stay assert after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.
- Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'
- CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
- Cycling input power OFF for 1 second or more then ON shall reset all STATUS_ bits to '0'
- Systems with redundant power supplies where only one of the supplies cycle input power OFF/ON; the power cycled PSU shall reset the STATUS_ bits to '0' only when powered back ON. If the PSU is kept OFF, the STATUS_ bits shall not be reset.

Default Limits for warning and faults

Warning limits shall be set with enough margin to guarantee no false warnings will occur is PSU operates within the specified requirements, but before the PSU shuts down. Fault limits shall be set at limits equal to or greater than the level at which the PSU shuts down.

Resetting to default limits

The PSU shall reset the warning and fault limits to default values for the following case.

- Input power cycling
- PSON power cycling

Faults and Error Checking

The PSU shall support PEC per the SMBus 2.0 specification.

Packet Error Checking

The PSU shall support packet error checking to support error checking and handling.

Capability and inventory reporting

The follow commands shall be supported for discovery of the power supplies capabilities.

Table 39 PMBus PSU Capability & Inventory Commands Summary

PMBus command	Value	Description
CAPABILITY	PEC = supported Bus speed = 100kHz SMBAlert# = supported	Defines the power supplies PEC support, bus speed, and support of SMBAlert#
QUERY	Linear formats for all but READ_EIN / READ_EOUT which is Direct	Used to determine if the PSU supports a specific command; It should return the proper information about any commands listed in the QUERY command.
PMBUS_REVISION	0010 0010	Used to verify the PMBUS_REVISION the PSU is based on. This shall be set to revision 1.2.
MFR_MAX_TEMP1	Trip threshold for the ambient temperature sensor (TEMP1) to assert	Defines the maximum inlet temperature to generate a warning condition in the STATUS_TEMPERATURE command.

	SMBAlert#	
MFR_MAX_TEMP2	Trip threshold for the hot spot temperature sensor (TEMP2) to assert SMBAlert#	Defines the maximum hotspot temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_IOUT_MAX	Rated output current using the linear format	Defines the maximum rated output current on the +12V rail.
MFR_POUT_MAX	Rated output power using the linear format	Defines the maximum rated output power of the PSU.
APP_PROFILE_SUPPORT	05h	Defines that the PSU supports this application profile.

SMBAlert#

The SMBAlert# signal may be asserted by the PSU for any of the supported STATUS events.

The events that control SMBAlert# can be masked using the SMBALERT#_MASK command. Default masking is shown in Status commands.

By default the SMBAlert# signal is asserted for the following cases.

1. STATUS_INPUT (UV Fault bit): input voltage drops below the fault threshold of the PSU for > 2ms.
2. STATUS_IOUT (Iout OC Warning bit): Output current exceeds the PSU capability but PSU has not shutdown.
3. STATUS_TEMPERATURE (OT Warning): Thermal sensor for PS inlet temperature or on a hot spot inside the PSU has exceeded its warning temperature.
4. STATUS_IOUT (Pout OP Warning bit): Output power exceeds the PSU capability but PSU has not shutdown.

Table 40 PSU SMBAlert# Timing Requirements

Item	Description	PMBus command	MIN	MAX
T_{alert_input}	Timing from input voltage dropping to 0VAC toSMBAlert# going low	STATUS_INPUTUV Fault		2 msec
$T_{OC\_Warning}$	Timing from output over current warning to SMBAlert# going low	STATUS_IOUT	10 msec	20 msec *
$T_{OC\_Warning\_latch}$	Time the PSU holds the SMBAlert# signal asserted after an over current warning event	STATUS_IOUT		30sec
T_{over_temp}	Hot spot temp > warning threshold	STATUS_TEMPERATURE Over temp warning		1 sec
$T_{smbalert\#\_shutdown}$	Minimum time PSU must continue to operate within voltage regulation limits and PWOK asserted after the SMBAlert# signal has been asserted due to an over temperature event.	NA	1sec	
$T_{max\_warning}$	Hot spot temperature inside the PSU that causes SMBAlert# to assert.	MFR_TEMP2_MAX	Tmax continuous	Tshutdown
$T_{OP\_Warning}$	Timing from output over power warning to SMBAlert# going low	STATUS_IOUT	100 μsec	

*This time must be shorter than OCP trip delay.
*2 msec Max Talert_input only applies to load higher than 10% of the rated load where SmaRT is meaningful.

SMBAlert# operation in standby mode

The PSU shall assert the SMBAlert# signal only when the main outputs are ON. SMBAlert# shall stay de-asserted when the PSU is in standby mode.

SMBALERT#_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT#_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits. The SMBALERT#_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

Reading mask values using PAGE_PLUS Block Write – Block Read Process Call with PEC

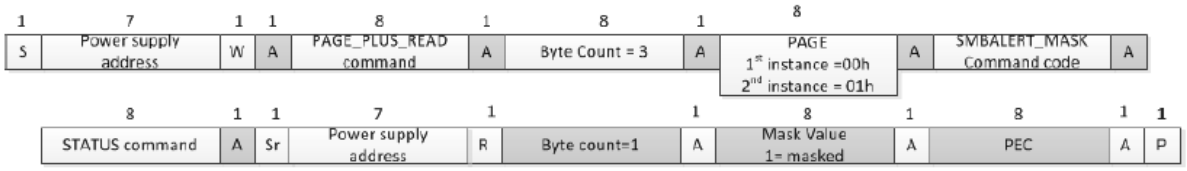

Figure 10 PAGE_PLUS_READ command

Writing mask values using PAGE_PLUS Block Write with PEC

STATUS_WORD is not used with SMBALERT#_MASK. Only the 'root' event bits are used to control the SMBAlert# Signal.

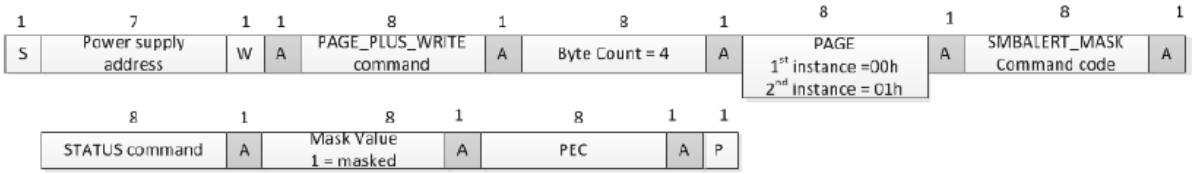

Figure 11 PAGE_PLUS_WRITE command.

Alert Response Address (ARA)

The power supply shall not support ARA. After asserting the SMBAlert# signal the power supply shall keep its address at it standard address; not change to 18h.

Setting and Resetting the SMBAlert# signal

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred.
This is a level detected event. Whenever the event is present SMBAlert# shall be asserted.
The SMBAlert# signal shall not de-assert at any time if the event that has caused the assertion is still present.
The SMBAlert# signal shall be cleared and re-armed by the following methods.

Clearing STATUS bits causing the asserted SMBAlert# signal. Power cycling.
with PSON or with input power Masking the event with SMBALERT#_MASK

Fan Speed Control

The PSU shall support the PMBus commands to allow the system to control and monitor the PSU's fan.

FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command.

This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU commands.The control is configured to be duty cycle controlled using the linear format of the PMBus protocol. The exponent N is fixed to a value of 0 (N = 0).

READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the PMBus linear format.

O T_WARN_LIMIT (51h)

The two data bytes are formatted in the Linear Data format. This may be used by the system test FW to simulate an assertion of the SMBAlert# signal due to a temperature warning event. This value shall be reset to the default value with any input power cycle or PSON power cycle.

IOUT_OC_WARN_LIMIT (4Ah)

The two data bytes are formatted in the Linear Data format.

PMBUS_REVISION

This is a correction to the table in the PMBus part II specification regarding the PMBUS_REVISION command.

Table 41 PMBUS_REVISION Command

Bits [7:4]	Part I revision	Bits [3:0]	Part II Revision
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

Continuous Assertion After Clearing If Condition Is Still Present

If the warning or fault condition is present when a bit is cleared, the bit and associated SMABLERT# signal stays asserted with no momentary transition to a de-asserted state.

10.2 Closed Loop System Throttling (CLST)

The power supply shall always assert the SMBAlert# signal whenever any component in the power supply reaches a warning threshold. Upon reduction of the load within 2msec after the SMBlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply shall continue to operate and not shutdown.

CLST Timing requirement

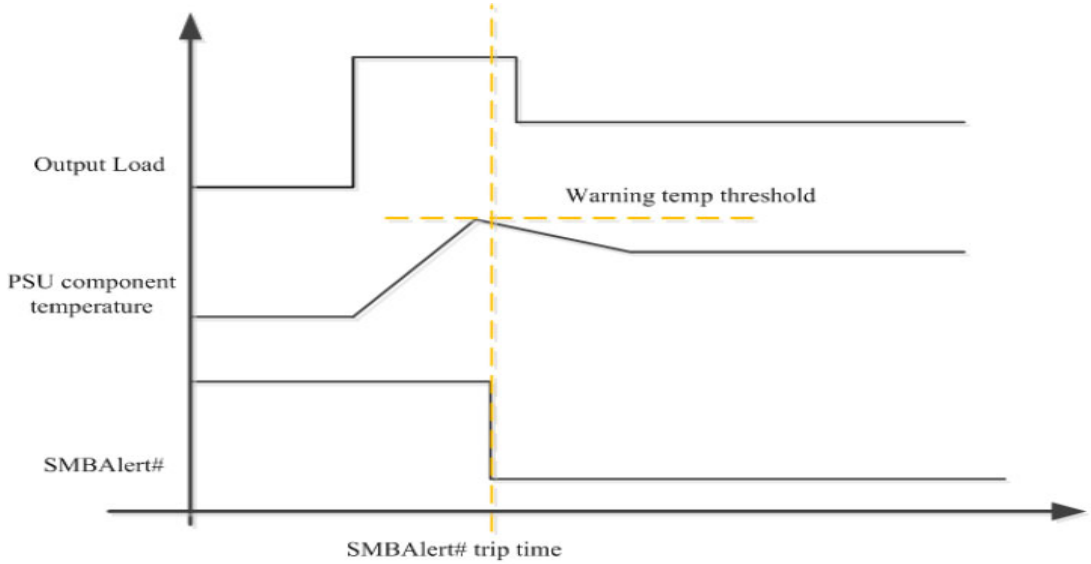

Figure 12 CLST Timing Requirement

10.3 Smart Ride-Through (SmaRT)

The power supply shall assert the SMBAlert# signal within 4msec after AC input voltage is lost to 0VAC.

10.4 Cold Redundancy

This is a common specification defining Cold Redundancy 2 requirements uses in redundant power supplies. It covers both power supply and system requirements supporting redundant configurations of 1+1, 2+2, and 3+1. Cold Redundancy uses the PMBus manufacturer specific command area to define SMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Cold Standby Power Supply Operating State

A power supply is put into Cold Standby whenever PSON# is asserted, CR_ON# is de-asserted, and COLD_RED_CONFIG value is set to 02h, 03h, or 04h. In the cold standby mode the power supply must:

Power ON when Cold_Red bus is driven LOW.

Turn off its output or'ing FET

Keep its internal output capacitor before the output or'ing FET charged to not less than 12.6V Keep PWOK asserted
Disconnect any output dummy loads to prevent discharging of the recharged output capacitor Power off any internal fans
Pre-bias its voltage error amplifier to maximum duty cycle (preventing the loop compensation from slowing up the turn on process)
Disable its output slow start circuit
Keep the PFC stage ON at lowest possible operating frequency and its output bulk capacitor charged
No PMBus fault or warning conditions reported via STATUS commands

Powering on Cold Standby supplies to maintain best efficiency

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at. The CR_BUS of any power supply may be in one of three different states; pulled low, pulled high, or tri-stated. In tri-state the CR_BUS is a high impedance to ground; only a high impedance resistor pulling the signal to ground.

Table 42 Example Load Share Threshold for Activating Supplies

	Enable Threshold for VCR_ON_EN	**Disable Threshold for VCR_ON_DIS**	**CR_BUS De-asserted / Asserted States**
Standard Redundancy	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1(02h)	3.2V (40% of max)	90% x (3.2V x 1/2) = 1.44V	OK = Tri-state Fault = Low
Cold Standby 2(03h)	5.0V (62% of max)	90% x (5.0V x 2/3) = 3.01V	OK = Tri-state Fault = Low
Cold Standby 3(04h)	6.7V (84% of max)	90% x (6.7V x 3/4) = 4.52V	OK = Tri-state Fault = Low

Note: Maximum load share voltage = 8.0V at 100% of rated output power These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve that specific model.

Cold Redundancy SMBus Commands

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. We will call the command Cold_Redundancy_Config (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

The power supplies setup to be the cold standby power supplies; shall change to standard redundancy mode (D0h = 00h) whenever the CR_BUS is pulled low.

Table 43 Redundancy Command Data

Cold_Redundancy_Config (D0h)		
Value	**State**	**Description**
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be

		in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active 1	Defines this power supply to be the one that is always ON in a cold redundancy
02h	Cold Standby 1	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.

Power Supply Turn On Function

Powering on and off of the cold standby power supplies is only controlled by each PSU sensing the Vshare bus. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the 'position' of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

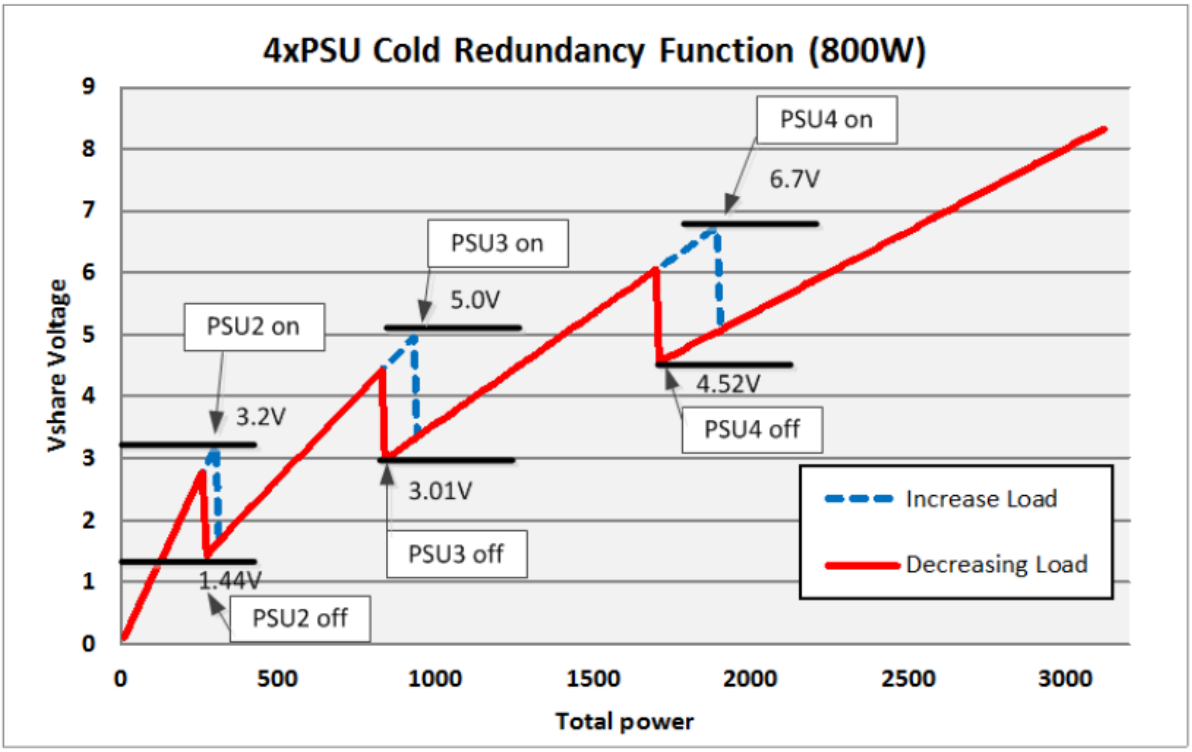

Figure 13 Example Power On/Off of power supplies in Cold Redundant Mode (4x800W PSUs)

10.5 Summary of SMBus/PMBus Commands

Table 44 Summary of SMBus/PMBus Commands

Command Code	Command Name	Transaction Type	Comment
00h	PAGE	R/W Byte	Switch PAGE PAGE value: 00h (BMC)

			PAGE value: 01h (ME) PAGE value: FFh (BMC & ME)
01h	OPERATION	R/W Byte	Reference Table 45
02h	ON_OFF_CONFIG	R/W Byte	Reference Table 46
03h	CLEAR_FAULTS	Send Byte	Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'. CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
05h	PAGE_PLUS_WRITE	Block Write	Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML.
06h	PAGE_PLUS_READ	Block Write–Block Read Process Call	The PAGE_PLUS_READ command is used for all read accesses of the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML registers at each of the system instances. Each instance is set by the same events but cleared by their own system master be it the PAGE 00h BMC or PAGE 01h ME.
19h	CAPABILITY	Read Byte	Defines the power supplies PEC support, bus speed, and support of SMBAlert#. PEC = supported Bus speed = 100kHz SMBAlert# = supported
1Ah	QUERY	Block Write–Block Read Process Call	The QUERY command is used to ask a PMBus device if it supports a given command, support write or support read only. This command used the Block Write-Block Read Process Call described in the version 2.0 SMBus specification.
1Bh	SMBALERT#_MASK	Write Word/ Block Write-Block Read Process Call	The SMBALERT#_MASK command controls which PSU STATUS_ event may trigger the SMBALERT# system interrupt signal.
20h	VOUT_MODE	Read Byte	Bits[7:5]: 000 (Linear format) Bits[4:0]: 10111 (N= -9, Exponent) 17h (n=-9)
30h	COEFFICIENTS	Block Write–Blo	M=01h, b=00h, R=00h Used to retrieve the m, b and R

		ck Read Process Call	coefficients for Interpreting READ_EIN and READ_EOUT command DIRECT format data only.
3Ah	FAN_CONFIG_1_2	Read Byte	Fan 1 is commanded in duty. The FAN_CONFIG_1_2 command must be set according to the requirements set by the PMBus specification. Fanless PSUs should respond appropriately. A returned value of 91h indicates fan in position one, commanded by % duty cycle and having 2 tach pulse/rev.
3Bh	FAN_COMMAND_1	R/W Word	This command use to adjust the operation duty of FAN. This command has two data bytes formatted in Linear-11 data format.
46h	IOUT_OC_FAULT_LIMIT (optional)	Read Word	The command sets the value of the output current measured at the sense or output pins that causes an output current fault. This value shall be reset to the default value with any input power cycle or PSON power cycle.
4Ah	IOUT_OC_WARN_LIMIT	Read Word	The command sets the value of the output current measured at the sense or output pins that causes an output over current warning. This value shall be reset to the default value with any input power cycle or PSON power cycle. Linear-11 data format.
51h	OT_WARN_LIMIT	Read Word	The command sets the value of temperature measured at the sense or pin that cause an over temperature warning. Linear-11 data format.
5Dh	IIN_OC_WARN_LIMIT	Read Word	Linear-11 data format.
6Ah	POUT_OP_WARN_LIMIT	Read Word	Linear-11 data format.
6Bh	PIN_OP_WARN_LIMIT	Read Word	Linear-11 data format
78h	STATUS_BYTE	Read Byte	This command returns one bytes of information with a summary of the unit's fault condition
79h	STATUS_WORD	Read Word	This command returns two bytes of information with a summary of the unit's fault condition
7Ah	STATUS_VOUT	Read Byte	BIT7:VOUT_OV_FAULT BIT4:VOUT_UV_FAULT
7Bh	STATUS_IOUT	Read Byte	BIT7 Iout OC fault BIT5 Iout OC warning BIT1 Pout OP fault BIT0 Pout OP warning

7Ch	STATUS_INPUT	Read Byte	
7Dh	STATUS_TEMPERATURE	Read Byte	BIT7:OTF (vendor define) BIT6:OTW (vendor define)
7Eh	CML	Read Byte	
81h	STATUS_FANS_1_2	Read Byte	
86h	READ_EIN	Block Read	
87h	READ_EOUT	Block Read	
88h	READ_VIN	Read Word	Linear-11 data format
89h	READ_IIN	Read Word	Linear-11 data format.
8Bh	READ_VOUT	Read Word	Linear-16 data format
8Ch	READ_IOUT	Read Word	Linear-11 data format.
8Dh	READ_TEMPERATURE_1	Read Word	Ambient Linear-11 data format
8Eh	READ_TEMPERATURE_2	Read Word	Secondary side (Hot Spot) Linear-11 data format.
8Fh	READ_TEMPERATURE_3	Read Word	Primary side (Hot Spot) Linear-11 data format.
90h	READ_FAN_SPEED_1	Read Word	Linear-11 data format.
96h	READ_POUT	Read Word	Linear-11 data format.
97h	READ_PIN	Read Word	Linear-11 data format
98h	PMBUS_REVISION	Read Byte	PMBus 1.2
99h	MFR_ID	Block Read	
9Ah	MFR_MODEL	Block Read	
9Bh	MFR_REVISION	Block Read	
9Ch	MFR_LOCATION	Block Read	
9Dh	MFR_DATE	Block Read	
9Eh	MFR_SERIAL	Block Read	
9Fh	APP_PROFILE_SUPPORT	Read Byte	05h Defines that the PSU supports this application profile
A0h	MFR_VIN_MIN	Read Word	90V Linear-11 data format.
A1h	MFR_VIN_MAX	Read Word	264V Linear-11 data format.
A2h	MFR_IIN_MAX	Read Word	Linear-11 data format.
A3h	MFR_PIN_MAX	Read Word	Linear-11 data format.
A4h	MFR_VOUT_MIN	Read Word	Linear-16 data format.
A5h	MFR_VOUT_MAX	Read Word	Linear-16 data format.
A6h	MFR_IOUT_MAX	Read Word	Linear-11 data format.
A7h	MFR_POUT_MAX	Read Word	800W Linear-11 data format.
A8h	MFR_TAMBIENT_MAX	Read Word	55 degree C Linear-11 data format.
A9h	MFR_TAMBIENT_MIN	Read Word	0degC Linear-11 data format.
ABh	MFR_EFFICIENCY_HL	Block Read	230VAC (20% of 800W) (50% of 800W) (100% of 800W) Linear-11 data format.
C0h	MFR_MAX_TEMP_1	Read Word	Inlet ambient warning temperature

			value Linear-11 data format.
C1h	MFR_MAX_TEMP_2	Read Word	Secondary hotspot warning temperature value Linear-11 data format.
C2h	MFR_MAX_TEMP_3	Read Word	Primary hotspot warning temperature value Linear-11 data format.
C3h	MFR_FAN_SPEED_MAX	Read Word	Return the maximum fan speed Linear-11 data format.
C4h	MFR_FAN_SPEED_MIN	Read Word	Return the minimum fan speed Linear-11 data format.
D0h	MFR_COLD_REDUNDANCY_CONFIG	Read/Write Byte	
D4h	MFR_HW_COMPATIBILITY	Read Word	Bootloader
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte	Bootloader
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte	Bootloader
D7h	MFR_FWUPLOAD		Bootloader
D8h	MFR_FWUPLOAD_STATUS	Block Write	Bootloader
D9h	MFR_FW_REVISION	Block Read	Bootloader
DCh	MFR_BLACKBOX	Block Read	Black Box
DDh	MFR_REAL_TIME_BLACK_BOX	Block Write/ Read	Black Box
DEh	MFR_SYSTEM_BLACK_BOX	Block Write/ Read	Black Box
DFh	MFR_BLACKBOX_CONFIG	Read/Write Byte	Black Box
E0h	MFR_CLEAR_BLACKBOX	Send Byte	Black Box

0x00h PAGE

The page command provides the ability to configure, control and monitor on multiple outputs through only one physical address. Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command. There is one data byte shown in table.

Table 45 PAGE

Value	Page #	Meaning
00h	0	Provide the data for BMC.
01h	1	Provide the data for ME.
FFh	All pages	Provide all the pages data.

0x01h OPERATION

The power on default condition of the PSU is ON. There is one data byte shown in table.

Table 46 OPEARTION

Value	Meaning
00h	Power off.
80h	Power on.

0x02h ON_OFF_CONFIG Command

ON_OFF_CONFIG command Default value is 0x1Dh.

Table 47 ON_OFF_CONFIG

Setting type	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Data value	Description[1]	Supported
1	0	X	X	X	1	0x01	If AC ok, turn-on power	YES
2	1	0	1	0	1	0x15	HW + LO	YES
3	1	1	0	X	1	0x19	SW	YES
4	1	1	1	0	1	0x1D	HW + LO + SW	YES

X = don't care HW = turn-on/off by control pin HI = control pin active high turn-on power LO = control pin active low turn-on power SW = turn-on/off by operation command.

0x03h CLEAR_FAULT

Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'. CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported. If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.

0x05h PAGE_PLUS_WRITE

0x06h PAGE_PLUS_READ

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Ex. Reading STATUS_WORD

Block Write – Block Read Process Call with PEC

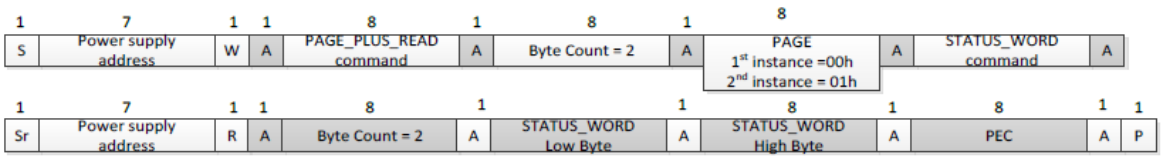

Figure 14 Reading STATUS_WORD Command with PAGE_PLUS_READ

Ex. Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML Block Write – Block Read Process Call with PEC

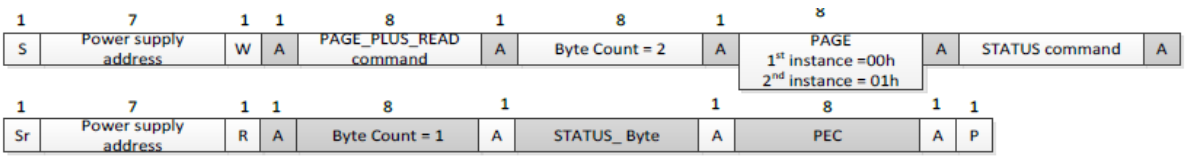

Figure 15 Reading STATUS Commands with PAGE_PLUS_READ

Ex. Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

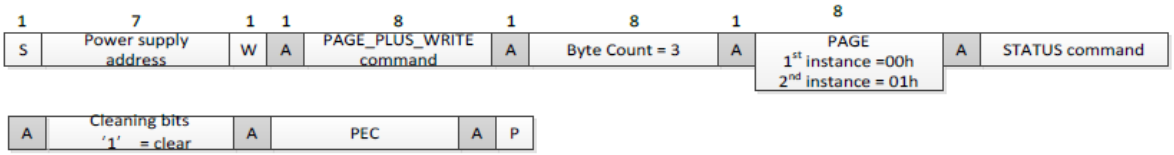

Figure 16 Clearing STATUS commands using PAGE_PLUS_WRITE

Note: STATUS_WORD cannot be cleared directly. It is cleared based on lower level status commands.

0x19h CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

Table 48 CAPABILITY

Bits	Description	Value	Meaning
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100kHz
		01	Maximum supported bus speed is 400kHz
		10	Reserved
		11	Reserved
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBUS Alert Response protocol
		1	The device does have a SMBALERT# pin and does support the SMBUS Alert Response protocol
3:0	Reserved	x	Reserved

0x1Ah QUERY

To ask a PMBUS device if it supports a given command, and if so, what data formats it supports for that command. This command use "Block Write-Block Read Process Call" to get the data.
Data definition is as shown in table.

Table 49 QUERY

Bits	Value	Meaning
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write

	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	xx	Reserved for future use

0x20h VOUT_MODE

This command defines the data formats for the output voltage and output voltage related parameters of a PMBUS device.

There is one data byte formatted as shown in table.

Table 50 VOUT_MODE

Bits	Description	Value	Meaning
7:5	Mode	000	Linear-16 data format mode.
4:0	Parameter N	xxxxx	N is a parameter for linear-16.

0x3Ah FAN_CONFIG_1_2

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM). 1 FAN is 0x90h.

Table 51 FAN_CONFIG_1_2

Bits	Value	Meaning
7	1	A Fan Is Installed In Position 1
	0	No Fan Is Installed In Position 1
6	1	Fan 1 Is Commanded In RPM
	0	Fan 1 Is Commanded In Duty Cycle
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution 00b = 1 pulse per revolution 01b = 2 pulses per revolution 10b = 3 pulses per revolution 11b = 4 pulses per revolution
3	1	A Fan Is Installed In Position 2
	0	No Fan Is Installed In Position 2
2	1	Fan 2 Is Commanded In RPM
	0	Fan 2 Is Commanded In Duty Cycle
1:0	00b-11b	Fan 2 Tachometer Pulses Per Revolution

0x3Bh FAN_COMMAND_1

The system may increase/decrease the power supplies fan speed through using the FAN_COMMAND_1 command. It can be increase/decrease by system command/FAN_COMMAND_1(3Bh) if the required fan duty is higher than PSU internal algorithm.

If the required fan duty is lower than internal algorithm, fan speed will reduce first. Then fan speed increase is based on internal algorithm. The control is configured to be duty cycle controlled using the linear format of the PMBus protocol.
The exponent N is fixed to a value of 0 (N = 0).

0x46h IOUT_OC_FAULT_LIMIT

The command sets the value of the output current measured at the sense or output pins that causes an output current fault. The two data bytes are formatted in the Linear11 Data format.

0x4Ah IOUT_OC_WARN_LIMIT

The command sets the value of the output current measured at the sense or output pins that causes an output over current warning. The two data bytes are formatted in the Linear11 Data format.

0x51h OT_WARN_LIMIT

The command sets the value of temperature measured at the sense or pin that cause an over temperature warning.
The two data bytes are formatted in the Linear11 Data format.

0x78h STATUS_BYTE

This command returns one byte of information with a summary of the unit's fault condition.
There is one data bytes formatted as shown in table.

Table 52 STATUS_BYTE

Byte	Bit	Name	Meaning
Low	7	BUSY	PSU must always respond and cannot say busy
	6	OFF	OFF = 1 when PWOK = 0 OFF = 0 when PWOK = 1
	5	VOUT_OV_FAULT	An output overvoltage fault has occurred
	4	IOUT_OC_FAULT	An output over current fault has occurred
	3	VIN_UV_FAULT	An input under voltage fault has occurred.
	2	TEMPERAUTRE	A temperature fault or warning has occurred
	1	CML	If any bits is asserted in STATUS_CML. Refer to STATUS_CML.
	0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] has occurred. If any 79h high byte bit asserted. NON OF THE ABOVE assert 1

0x79h STATUS_WORD

This command returns two bytes of information with a summary of the unit's fault condition.
There is two data bytes formatted as shown in table.

Table 53 STATUS_WORD

Byte	Bit	Name	Meaning
Low	7	BUSY	PSU must always respond and cannot say busy.
	6	OFF	This bit is asserted if the unit is not providing power to the output. Refer to VOUT_UV_FAULT.

	5	VOUT_OV_FAULT	An output overvoltage fault has occurred. Refer to VOUT_OV_FAULT.
	4	IOUT_OC_FAULT	An output over current fault has occurred. Refer to IOUT_OC_FAULT.
	3	VIN_UV_FAULT	An input under voltage fault has occurred. Refer to VIN_UV_FAULT.
	2	TEMPERAUTRE	A temperature fault or warning has occurred. Refer to OT_FAULT or OT_WARN. (Hotspot)
	1	CML	If any bits is asserted in STATUS_CML. Refer to STATUS_CML
	0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] has occurred.
High	7	VOUT	An output voltage fault has occurred. Refer to STATUS_VOUT
	6	IOUT/POUT	An output current or output power fault has occurred. Refer to STATUS_IOUT.
	5	INPUT	An input voltage fault has occurred. Refer to STATUS_INPUT
	4	MFR_SPECIFIC	Reserved.
	3	POWER_GOOD#	The POWER_GOOD signal, if present, is negated. 1: PSU failed. 0: PSU ok.
	2	FANS	A fan fault or warning has occurred. Refer to STATUS_FAN_1_2.
	1		Reserved
	0		Reserved

0x7Ah STATUS_VOUT

This command returns one data byte with contents as below table.

Table 54 STATUS_VOUT

Bits	Name	Meaning
7	VOUT_OV_FAULT	Output over voltage fault.
6:5		Reserved
4	VOUT_UV_FAULT	Output under voltage fault.
3:0		Reserved.

0x7Bh STATUS_IOUT

This command returns one data byte with contents as below table.

Table 55 STATUS_IOUT

Bits	Name	Meaning
7	Iout OC fault	Output over current fault.
6		Reserved
5	Iout OC warning	Output over current warning.
4:3		Reserved
1	Pout OP fault	Output over power fault.
0	Pout OP warning	Output over power warning.

0x7Ch STATUS_INPUT

This command returns one data byte with contents as below table

Table 56 STATUS_INPUT

Bits	Name	Meaning
7	VIN_OV_FAULT	Input over voltage fault.
6	VIN_OV_WARN	Input over voltage warning.
5	VIN_UV_WARN	Input under voltage warning.
4	VIN_UV_FAULT	Input under voltage fault.
3	VIN_LOW_OFF	Keep the same as under voltage fault. Refer to VIN_UV_FAULT.
2		Reserved.
1	IIN_OC_WARNING	(Input Over current Warning) Iin OC warning
0	IN_OP_WARNING	(Input Over power Warning) Pin OP warning

0x7Dh STATUS_TEMPERATURE

This command returns one data byte with contents as below table

Table 57 STATUS_TEMPERATURE

Bits	Name	Meaning
7	OT_FAULT	Over temperature fault. (Hotspot)
6	OT_WARN	Over temperature warning. (Hotspot)
5:0		Reserved.

0x7Eh STATUS_CML

This command returns one data byte with contents as below table.

Table 58 STAUTS_CML

Bits	Name	Meaning
7	INVALID_CMD	Invalid or unsupported command received.
6	INVALID_DATA	Invalid or unsupported data received.
5	PEC_FAULT	Packet error check failed.
4:0		Reserved.

0x81h STATUS_FANS_1_2

This command returns one data byte with contents as below table.

Table 59 STATUS_FAN_1_2

Bits	Name	Meaning
7	FAN1_FAULT	Fan fault.
6	FAN2_FAULT	No fan2
5	FAN1_WARN	Fan warning.
4	FAN2_WARN	No fan2
3:0		Reserved

0x86h READ_EIN

The READ_EIN command is used to return information the host can use to calculate the input power consumption of a PMBus device. The information provided by this command is independent of any device specific averaging period, sampling frequency or calculation algorithm. A value of 0 should be returned when no input line present. Refer to the prior definition for the detail.

0x87h READ_ EOUT

The READ_EOUT command is used to return information the host can use to calculate the input power consumption of a PMBus device. The information provided by this command is independent of any device specific averaging period, sampling frequency or calculation algorithm. A value of 0

should be returned when no input line present. Note that the averaging period requirements differ depending upon whether the PSU is an AC input type. Refer to the prior definition for the detail.

0x88h READ_ VIN

This command returns the input voltage in volts. It returns two data bytes which are formatted in the linear-11 data format.

0x89h READ_ IIN

This command returns the input current in amps. It returns two data bytes which are formatted in the linear-11 data format.

0x8Bh READ_VOUT

This command returns the output voltage in volts. It returns two data bytes which are formatted in the linear-16 data format. Linear 16 data need to refer the 0x20 VOUT_MODE's N format.

0x8Ch READ_ IOUT

This command returns the output current in amps. It returns two data bytes which are formatted in the linear-11 data format.

0x8Dh READ_TEMPERATURE_1

This command returns the ambient temperature in degree Celsius. It returns two data bytes which are formatted in the linear-11 data format. N=0.

0x8Eh READ_TEMPERATURE_2

This command returns the max temperature of primary side in degree Celsius. It returns two data bytes which are formatted in the linear-11 data format. N=0.

0x8Fh READ_TEMPERATURE_3

This command returns the max temperature of secondary side in degree Celsius. It returns two data bytes which are formatted in the linear-11 data format. N=0.

0x90h READ_FAN_SPEED_1

This command returns the fan speed in RPM. It returns two data bytes which are formatted in the linear-11 data format.

0x96h READ_POUT

This command returns the output power in watts. It returns two data bytes which are formatted in the linear-11 data format.

0x97h READ_PIN

This command returns the output power in watts. It returns two data bytes which are formatted in the linear-11 data format.

0x98h PMBUS_REVISION

This command returns the revision of PMBUS specification to which the device is compliant. There is

one data byte shown in table

Table 60 PMBUS_REVISION

Value	Meaning
22h	PMBUS specification 1.2

0x99h MFR_ID

This command is used to read the manufacturer's ID. There is multi-data byte shown in table.

Table 61 MFR_ID

Byte Number	Value	Meaning
14	Great Wall	ASCII code.

0x9Ah MFR_ MODEL

This command is used to read the manufacturer's model name. There is multi-data byte shown in table

Table 62 MFR_MODEL

Byte Number	Value	Meaning
14	GW-CRPS800N2	ASCII code.

0x9Bh MFR_ REVISION

This command is used to read the manufacturer's revision number. There is multi-data byte shown in table

Table 63 MFR_REVISION

Byte Number	Value	Meaning
6	XXX	HEX.

0x9Ch MFR_LOCATION

This command is used to read the manufacturing location of the PSU. There is multi-data byte shown in table.

Table 64 MFR_LOCATION

Byte Number	Value	Meaning
20	SHENZHEN CHINA	ASCII code

0x9Dh MFR_ DATE

This command is used to read the date the PSU was manufactured. The format is YYMMDD where Y, M and D are integer values from 0 to 9. There is multi-data byte shown in table.

Table 65 MFR_DATE

Byte Number	Value	Meaning
0:1	YY	Year
2:3	MM	Month
4:5	DD	Day

0x9Eh MFR_ SERIAL

This command is used to read the manufacturer's serial number. There is multi-data byte shown in table.

Table 66 MFR_SERIAL

Byte Number	Value	Meaning
14	XXX	ASCII codes.

0x9Fh APP_PROFILE_SUPPORT

Defines that the PSU supports this application profile

0xA0h MFR_VIN_MIN

This command returns the minimum rated value, in volts, of input voltage.

0xA1h MFR_VIN_MAX

This command returns the maximum rated value, in volts, of input voltage.

0xA2h MFR_IIN_MAX

This command returns the maximum rated value, in amps, of input current.

0xA3h MFR_PIN_MAX

This command returns the maximum rated value, in watts, of input power.

0xA4h MFR_ VOUT_MIN

This command returns the minimum rated value, in volts, of output voltage.

0xA5h MFR_ VOUT_MAX

This command returns the maximum rated value, in volts, of output voltage.

0xA6h MFR_ IOUT_MAX

This command returns the maximum rated value, in amps, of output current.

0xA7h MFR_ POUT_MAX

This command returns the maximum rated value, in watts, of output power.

0xA8h MFR_ TAMBIENT _MAX

This command returns the maximum rated ambient temperature, in degrees Celsius.

0xA9h MFR_ VOUT_MAX

This command returns the minimum rated ambient temperature, in degrees Celsius.

0xABh MFR_EFFICIENCY_HL

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input

voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. Each value (voltage, power or efficiency) is transmitted as two bytes in Linear format.

Table 67 MFR_EFFICIENCY_HL

Byte Number	Byte Order.	Description
0	Low Byte	The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified.
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte
13	High Byte	

10.6 In-System Firmware Upload

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the OFF state.

FW Image Mapping

The power supply firmware image shall be made up of two parts; 1)Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1. Boot Loader: This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power OFF into the boot loader mode no matter the state of the power supply's main program.

2. Main Program: This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

Summary of Commands & Capabilities supported in Boot Loader mode

When the power supply is in FW Upload mode the following commands shall be supported

Table 68 Summary of Commands & Capabilities supported in Boot Loader mode

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte w/PEC
1Ah	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC
98h	PMBUS_REVISION	Read Byte w/PEC

9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	MFR_FWUPLOAD	Block Write w/ PEC (size = block size from image header)
D8h	MFR_FWUPLOAD_STATUS	Read Word w/PEC
D9h	MFR_FW_REVISION	Block Read w/PEC (3 bytes)

LED Status

While the PSU FW image is being updated the PSU shall blink the Green LED at a 2Hz rate.

Power supply may be able to support FW upload in the OFF state. The new FW will take effect once it is taken out of FW upload load.

Bad image after firmware update:

The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

Table 69 Firmware Image Header

Byte 1	CRC LowByte
Byte 2	CRC HighByte
Byte 3	Image Information
Byte 4	Image Information
Byte 5	Image Information
Byte 6	Image Information
Byte 7	Image Information
Byte 8	Image Information
Byte 9	Image Information
Byte 10	Image Information
Byte 11	X
Byte 12	X
Byte 13	X
Byte 14	X
Byte 15	X
Byte 16	X
Byte 17	X
Byte 18	X
Byte 19	X
Byte 20	X
Byte 21	X
Byte 22	
Byte 23	
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).
Byte 25	FW_MINOR_PRIMARY (not used by system)
Byte 26	FW_MINOR_SECONDARY
Byte 27	HW_COMPATIBILITY_FIRST
Byte 28	HW_COMPATIBILITY_SECOND
Byte 29	BLOCK SIZE LowByte
Byte 30	BLOCK SIZE HighByte
Byte 31	Write Time LowByte
Byte 32	Write Time HighByte

Byte11~Byte23 vendor define model name area.

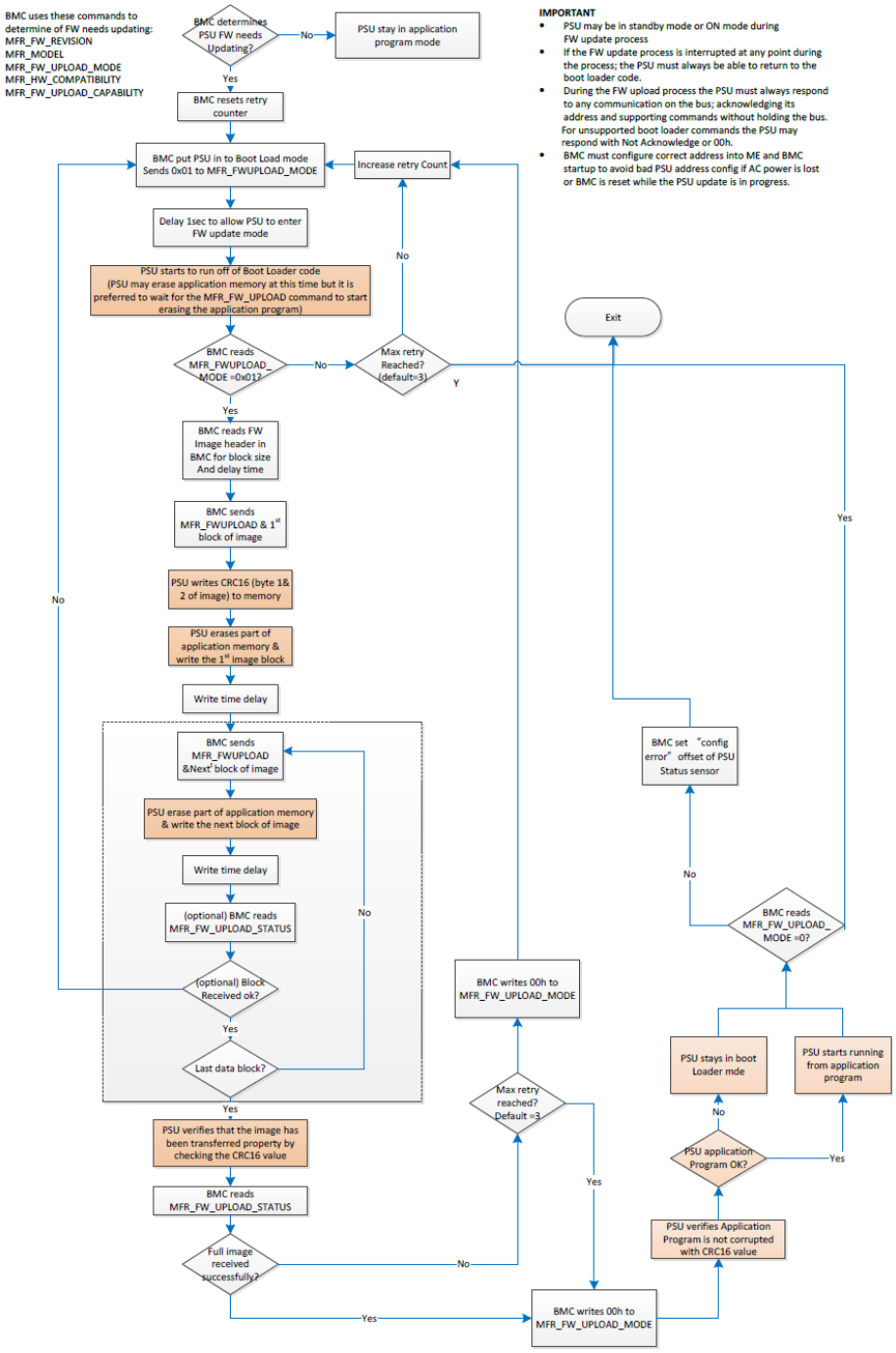

Figure 17 PSU Upload Process

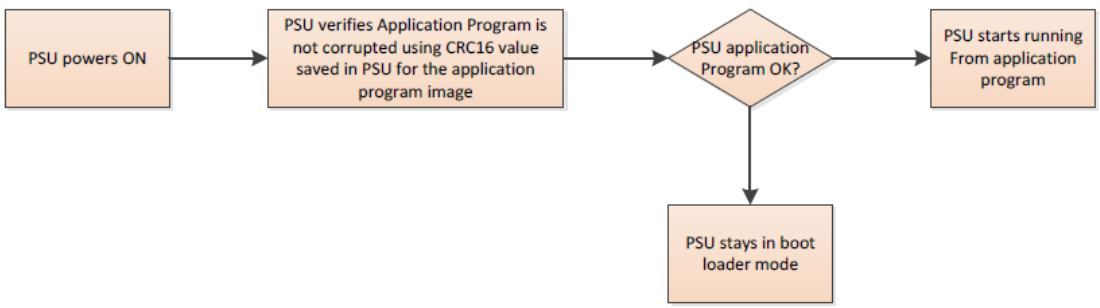

Figure 18 PSU flow during powering ON

Power supply commands

Name: MFR_HW_COMPATIBILITY

Format: Read Word

Code: D4h

Table 70 MFR_HW_COMPATIBILITY

Bytes	Value	Description
low	ASCI code for first letter/number of the PSU HW compatibility	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Table 71 MFR_FWUPLOAD_CAPABILITY

Bit	Value	Description
0 (for future use)	1= PSU support FW uploading in standby mode only	For future use
1 (for future use)	1= PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	For future use
2	1= PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

Code: D6h

Table 72 MFR_FWUPLOAD_MODE

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7	Reserved	1-7

Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

Table 73 MFR_FWUPLOAD

Bytes	Value	Description
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 10.5.5. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process. Reset: all bits get reset to '0' when the power supply enters FW upload mode.

Table 74 MFR_FWUPLOAD_STATUS

Bit	Description
0	1= Full image received successfully
1	1= Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1= Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3(for future use)	1= Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1= FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: D9h

Table 75 MFR_FW_REVISION

Byte	Value	Description
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7=1 Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed, but recommended to follow. Bit 7=0 No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

MFR_MODEL (existing PMBus command)

Code: 9Ah

Maximum of 14 byte value; ending in terminator character

MFR_REVISION (existing PMBus command)

Code: 9Bh

10.7 Black Box

This specification defines the requirements for power supplies with PMBus capability to store PMBus

and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shut down. The data can be accessed via the PMBus interface by applying power to the +12VSB pins. No AC power needs to be applied to the power supply.

When data is saved to the Black Box?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

Black Box Events

There are two types of data saved in the black box; 1) System Tracking Data, 2) Power supply event data.

System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

Black Box Process

- System writes system tracking data to the power supply RAM at power ON
- System writes the real time clock data to the PSU RAM once every ~5 minutes
- Power supply tracks number of PSON and AC power cycles in EEPROM
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event; the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM.
- Upon a fault event that causes the PSU to shutdown all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

Commands

Name: MFR_BLACKBOX

Format: Read Block with PEC (238 bytes)

Code: DCh

Table 76 MFR_BLACKBOX

	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCI characters.

	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these times and power cycle counters in RAM. When the black box event occurs the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System(reserved for future use)	4	This time stamp does not need to generate by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from00:00:00, January 1, 1970. This format is sufficient to maintain time

			stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These values shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	

	Shutdown due to over voltage on output	Upper ½	asserted.
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

Name: MFR_REAL_TIME_BLACK_BOX
Format: Write/Read Block with PEC (4 bytes)
Code: DDh
The system shall use this command to periodically write the real time clock data to the power supply. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970.
This format is sufficient to maintain time stamping with 1-second resolution past the year 2100.
This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Name: MFR_SYSTEM_BLACK_BOX
Format: Write/Read Block with PEC (40 bytes). Low byte first
Code: DEh
The system uses this command to write the following data to the PSU.

Table 77 MFR_SYSTEM_BLACK_BOX

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

Name: MFR_BLACKBOX_CONFIG
Format: Read/Write Byte with PEC
Code: DFh

Table 78 MFR_BLACKBOX_CONFIG

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		reserved

Name: MFR_CLEAR_BLACKBOX
Format: Send Byte with PEC
Code: E0h

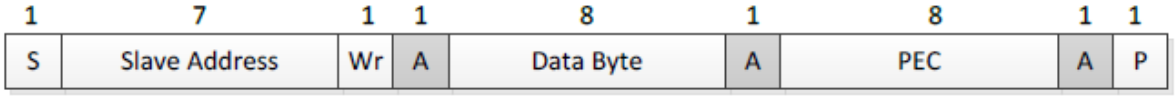

Figure 19 Send Byte protocol with PEC

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously. This command is written only. There is no data byte for this command.

Hardware Requirements

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied and power is only applied at the standby output pins by an external source (+12VSB).

11 Reliability

11.1 Component De-rating

Refer to latest version of GreatWall component derating guide. Any exceptions are subject to final approval.

11.2 Life Requirement

The power supply shall support 5 years calculated life with a 90% confidence under the following conditions:

- 100-240Vac input.
- 55°C inlet temperature.
- 20% of the time at 20% load; 80% of the time at 80% load.
- 900m altitude.

11.3 Mean Time Between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 250,000 hours at 75% load and 55°C, as calculated by Telcordia SR-332 Issues 2.

12 Product Safety And EMC Compliance

12.1 Product Safety Compliance

IEC60950-1 (International)
IEC62368-1 (International)
CE - Low Voltage Directive 2014/35/EU
GB4943.1

12.2 Product EMC Compliance – Class A Compliance

Note: The product is required to comply with Class A emission requirements.
EN55022 - Emissions (Europe)
EN55032 - Emissions (Europe)
EN55024 - Immunity (Europe)
EN55035 - Immunity (Europe)

- EN61000-4-2 Electrostatic Discharge
- EN61000-4-3 Radiated RFI Immunity
- EN61000-4-4 Electrical Fast Transients
- EN61000-4-5 Electrical Surge
- EN61000-4-6 RF Conducted Immunity
- EN61000-4-8 Power Frequency Magnetic Fields
- EN61000-4-11 Voltage Dips and Interruptions *EN61000-3-2 - Harmonics (Europe)

CE – EMC Directive 89/336/EEC (Europe)
GB 9254 - (EMC)
GB 17625.1 - (Harmonics)

12.3 Dielectric Withstand (Hi-pot)

12.3.1 Input to earth ground 1500Vac or 2250Vdc for 1 minute, less than 10mA leakage.
12.3.2 Primary to secondary 3000Vac or 4240Vdc for 1 minute, less than 30mA leakage.
12.3.3 Primary to secondary 500Vdc for 1 minute, isolation resistance shall not be less than 2Mohm.